PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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jc715 U.S. PTO 06/05/00

Attorney Docket No.: JAO 39894.01

Date: June 5, 2000

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BOX PATENT APPLICATION

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

CONTINUING APPLICATION TRANSMITTAL
RULE 1.53(b)

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is a

☐ Continuation ☒ Divisional ☐ Continuation-in-Part

application of prior pending Application No. 08/914,095, filed August 19, 1997,

For (Title): A SEMICONDUCTOR DEVICE AND A METHOD FOR MAKING THE SAME THAT PROVIDE ARRANGEMENT OF A CONNECTING REGION FOR AN EXTERNAL CONNECTING TERMINAL (AS AMENDED)

By (Inventors): Kazuo TANAKA

1. ☒ A Declaration and Power of Attorney is attached. The attached Declaration and Power of Attorney is:

   ☒ a. A copy of the Declaration and Power of Attorney from the parent application. (Used with the same or fewer inventors and (a) a copy of the prior application or (b) a revised, reformatted or edited version of the prior application that does not contain new matter.)

   ☐ b. A new Declaration and Power of Attorney. (Used with the same, fewer or additional inventors and (a) a copy of the prior application, (b) a revised, reformatted or edited version of the prior application that does not contain new matter, or (c) a new specification.)

2. ☒ The filing fee is calculated below:

CLAIMS IN THE APPLICATION AFTER ENTRY OF ANY PRELIMINARY AMENDMENT NOTED BELOW

FOR:	NO. FILED	NO. EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY FEE
BASIC FEE				$ 345	OR		$ 690
TOTAL CLAIMS	11 - 20	= *	x 9 =	$	OR	x 18	$
INDEP CLAIMS	2 - 3	= *	x 39 =	$	OR	x 78	$
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED			+130 =	$	OR	+260	$
			TOTAL	$	OR	TOTAL	$690

* If the difference is less than zero, enter "0".

3. ☒ Check No. 109083 in the amount of $690 to cover the filing fee is attached. The Director is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

4. ☐ Cancel claims _____of the application before calculating the filing fee. At least one independent claim is retained for filing purposes.

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

5. ☒ Amend the specification by inserting before the first line the sentence:

--This is a ☐ Continuation ☒ Division ☐ Continuation-in-Part of Application No. 08/914,095 filed August 17, 1997. The entire disclosure of the prior application is hereby incorporated by reference herein in its entirety.--

6. ☒ Formal drawings (Figs. 1-23) are attached.

7. ☒ Priority of foreign application No. 8-237310 filed August 20, 1999 in Japan is claimed under 35 U.S.C. §119 and/or §365(b).

☒ The certified copy was filed in prior Application No. 08/914,095 on November 7, 1997.

☐ A certified copy of the above foreign application(s) is filed herewith.

8. ☐ Priority of U.S. Provisional Application(s) No. _____ filed _____ is claimed under 35 U.S.C. §119.

☐ Amend the specification by inserting before the first line the sentence:

--This nonprovisional application claims the benefit of U.S. Provisional Application(s) No. _____ filed _____.--

9. ☒ The prior application is assigned of record to Seiko Epson Corporation recorded at Reel 8990, Frame 0989.

10. ☐ This application is filed by fewer than all the inventors named in the prior application (37 C.F.R §1.53(b)(1)). Delete the following inventor(s) named in the prior application:

11. ☒ A Preliminary Amendment is attached. Claims added by this Amendment are properly numbered consecutively beginning with the number next following the highest numbered claim in the application.

12. ☒ An Information Disclosure Statement is attached.

13. ☐ Small entity status:

☐ a. A small entity statement is attached.

☐ b. A small entity statement was filed in the parent application and such status is still proper and desired.

☐ c. Small entity status is no longer claimed.

14. ☐ Other: _____

15. ☒ The power of attorney in the application is to James A. Oliff, Registration No. 27,075, William P. Berridge, Registration No. 30,024, Kirk M. Hudson, Registration No. 27,562, Thomas J. Pardini, Registration No. 30,411, Edward P. Walker, Registration No. 31,450, Robert A. Miller, Registration No. 32,771, Mario A. Costantino, Registration No. 33,565, and/or Stephen J. Roe, Registration No. 34,463.

☐ a. The power appears in the attached Declaration and Power of Attorney.

☐ b. Since the power does not appear in the attached Declaration and Power of Attorney, a substitute Power of Attorney is also attached.

16. ☒ Address all future communications to:

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Respectfully submitted,

James A. Oliff
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JAO:TAD/lcw

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Kazuo TANAKA

Rule 1.53(b) Divisional of
Application No. 08/914,095

Filed: June 5, 2000 Docket No.: JAO 39894.01

For: A SEMICONDUCTOR DEVICE AND A METHOD FOR MAKING THE SAME THAT PROVIDE ARRANGEMENT OF A CONNECTING REGION FOR AN EXTERNAL CONNECTING TERMINAL (AS AMENDED)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the title to --A SEMICONDUCTOR DEVICE AND A METHOD FOR MAKING THE SAME THAT PROVIDE ARRANGEMENT OF A CONNECTING REGION FOR AN EXTERNAL CONNECTING TERMINAL--.

IN THE CLAIMS:

Please cancel claims 1, 9-11 and 15-20.

Please amend claims 2-4, 6-8 and 12-14 as follows:

2. (Amended) [The semiconductor device according to claim 1] A semiconductor device having a multiple wiring layer structure, comprising:

a first conductive layer connected to a conductive member for external connection;

a second conductive layer disposed below said first conductive layer the second conductive layer having a plurality of openings;

a third conductive layer disposed below said second conductive layer;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

a first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

a second through hole provided in said second insulating interlayer; and

a fifth conductive layer filling said second through hole, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of said first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer.

3. (Amended) The semiconductor device according to claim [1] 2, wherein said second conductive layer has a planar network pattern.

4. (Amended) [The semiconductor device according to claim 1] A semiconductor device having a multiple wiring layer structure, comprising:

a first conductive layer connected to a conductive member for external connection;

a second conductive layer disposed below said first conductive layer the second conductive layer having a plurality of openings;

a third conductive layer disposed below said second conductive layer;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

a first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

a second through hole provided in said second insulating interlayer; and

a fifth conductive layer filling said second through hole, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of said first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer, said third conductive layer is the lowest conductive layer formed on an insulating film covering a surface of a semiconductor substrate, and said third conductive layer is also provided with a plurality of openings.

6. (Amended) The semiconductor device according to claim [1] 2, wherein said conductive member for external connection is a bonding wire.

7. (Amended) The semiconductor device according to claim [1] 2, wherein said first conductive layer, said second conductive layer and said third conductive layer comprise aluminum as a major component, and said fourth conductive layer and said fifth conductive layer comprise tungsten as a major component.

8. (Amended) The semiconductor device according to claim [1] 2, wherein said semiconductor device further comprises an internal circuit, said internal circuit being formed by the multiple wiring layer structure, and said first conductive layer, said second conductive layer, said third conductive layer, said fourth conductive layer, said fifth conductive layer,

said first insulating interlayer, said second insulating interlayer, said through holes, and said multiple wiring layer structure are formed by a collective production process.

12. (Amended) The semiconductor device according to claim [1] 2, wherein the first and second through holes are axially aligned.

13. (Amended) The semiconductor device according to claim [1] 2, wherein the first and second through holes are axially offset.

14. (Amended) The semiconductor device according to claim [1] 2, wherein the fourth and fifth conductive layers do not overlap.

Please add claim 21 as follows:

--21. The semiconductor device according to claim 4, wherein the contiguous section is formed perpendicularly between said first conductive layer and said third conductive layer.--

REMARKS

Claims 2-8, 12-14 and 21 are pending. By this Amendment, the title is amended, claims 1, 9-11 and 15-20 are canceled, claims 2 and 4 are placed in independent form, claims 3, 6-8 and 12-14 are amended to depend from claim 2, and claim 21 is added for clarity. No new matter is added.

The December 3 Office Action in the parent application rejects claims 2, 3, 6, 8, 13 and 14 under 35 U.S.C. §102(e) over Chittipeddi et al. (U.S. Patent No. 5,751,065).

Applicant submits that Chittipeddi et al. does not disclose or suggest that the first insulating interlayer and the second insulating interlayer are connected to each other through the openings of the second conductive layer, in a contiguous section of the first insulating interlayer with the second insulating interlayer is, thereby, formed between the first conductive layer and the third conductive layer, as recited in claim 2. In fact, as admitted by the Office Action, the openings 307 of the middle layer 215 are merely for stress relief, and

thus, Chittipeddi et al. is unconcerned with connecting the dielectric layers provided thereon. Since the openings 307 of Chittipeddi et al. are for stress relief, the opening area may be very small. Thus, it becomes very difficult to fill the opening with insulating material to connect the layers through the openings when the opening area is very small.

Accordingly, claim 2 is not anticipated it by Chittipeddi et al. Because claims 3, 6, 8, 13 and 14 depend from claim 2, claims 3, 6, 8, 13 and 14 also are not anticipated by Chittipeddi et al.

The December 3 Office Action in the parent application rejects claims 1-8 and 12 under 35 U.S.C. §103(a) over Ito et al. (U.S. Patent No. 5,847,466) in view of Chittipeddi et al.

Applicant submits that Ito et al. does not disclose or suggest a first insulating interlayer and a second insulating interlayer connected to each other through openings of a second conductive layer, a contiguous section of the first insulating interlayer and the second interlayer, is, thereby, formed between a first conductive layer and third conductive layer, as recited in claims 2 and 4. In fact, as the Office Action admitted, Ito et al. does not disclose or suggest a second conductive layer and a third conductive layer having openings.

Furthermore, Chittipeddi et al. does not disclose or suggest these features of claims 2 and 4 missing from Ito et al. As discussed above, Chittipeddi et al. is unconcerned with connecting the dielectric layers. Accordingly, even if combined, Ito et al. and Chittipeddi et al. do not disclose or suggest the features of claims 2 and 4. Accordingly, claims 2 and 4, and claims 3, 5-8 and 12, depending from claim 2, would not have been obvious over Ito et al. and Chittipeddi et al.

For at least the above reasons, Applicant submits that claims 2, 3, 6, 8, 13 and 14 are not anticipated by Chittipeddi et al., and claims 2-8 and 12 would not have been obvious over Ito et al. and Chittipeddi et al.

Furthermore, Ito et al., Chittipeddi et al., and Hara et al., alone or in combination, do not disclose or suggest a contiguous section formed perpendicularly between said first conductive layer and said third conductive layer, as recited in new claim 21.

Applicant submits that the application is in condition for allowance. Prompt consideration and due allowance are earnestly solicited.

Should the Examiner believe anything further is desirable in order to place the Application in even better condition for allowance, the Examiner is requested to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Thu Anh Dang
Registration No. 41,544

Date: June 5, 2000

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SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to semiconductor devices and methods for making the same, and particularly, an electrode structure for connecting an external connecting terminal, such as a bonding wire, to an IC chip and a method for making the same.

2. Description of Related Art

A high density arrangement of electrodes (pads) for connecting external connecting terminals, such as a bonding wire, has been required due to the increasing integration density of ICs.

A cross-sectional view of a bonding pad formed using three layers of wiring is exemplified in Figure 23.

In a structure as shown in Figure 23, some problems, such as disconnection due to bumps of aluminum wiring and a narrowed bonding region, often arise.

Specifically, when superposing an aluminum pad 8010 as a first layer, an aluminum pad 8110 as a second layer and an aluminum pad 8310 as a third layer, the thickness of each aluminum layer decreases due to a steep slope between different levels, and disconnection due to bumps will readily occur. There is a fair possibility of disconnection due to bumps at a region surrounded with a chain-line circle 8500 in Figure 23.

The bonding region decreases with an increased number of electrode layers. As shown in the bottom side of Figure 23, the end of a region capable of bonding in the first pad layer 8010 is represented by P1, the end of a region capable of bonding in the second pad layer 8110 is represented by P2, the end of a region capable of bonding in the third pad layer 8310 is represented by P3, and thus a bonding region decreases as a new layer is superposed. When further superposition of the electrode layers is accelerated, the first electrode layer

therefore must have a large area in order to secure the bonding area, and it is difficult to arrange the bonding pad with high density.

SUMMARY OF THE INVENTION

The present invention has been completed in view of the above-mentioned problems, and it is an object of the present invention to provide a semiconductor device and a method for making the same which are capable of high density arrangement of the connecting region for an external connecting terminal, such as a bonding pad, and which are highly reliable.

The present invention which solves the above-mentioned problems has the following construction:

(1) The present invention described in claim 1 is characterized by a semiconductor device having a multiple wiring layer structure, comprising:

a first conductive layer belonging to a first layer and connected to a conductive member for external connection;

a second conductive layer belonging to a second layer below the first layer and provided with a plurality of openings;

a third conductive layer belonging to a third layer below the second layer;

a first insulating interlayer disposed between the first conductive layer and the second conductive layer;

a first through hole provided in the first insulating interlayer;

a fourth conductive layer filled in the first through hole;

a second insulating interlayer disposed between the second conductive layer and the third conductive layer;

a second through hole provided in the second insulating interlayer; and

a fifth conductive layer filled in the second through hole.

According to the claimed invention, the first to third conductive layers form a planar structure having no level differences. Thus, disconnection due to bumps will not occur. The bonding region of each layer always has a constant area in a multiple layer structure. High density bonding pad arrangement therefore can be achieved.

Herein, the term "second layer" means at least one layer of conductive layers (intermediate conductive layers) disposed between the first conductive layer and the third conductive layer.

Herein, "first and second layers" widely include, for example, oxide films, silicon nitride films, impurity containing oxide films, organic containing oxide films, insulating films comprising organic materials, and insulating films formed by superposing 2 or more types of the above-mentioned insulating films.

The second conductive layer is provided with openings, the first insulating interlayer and the second insulating interlayer are connected to each other through the openings, and a contiguous section of the insulating interlayer is, thereby, disposed between the first conductive layer and the second conductive layer. Namely, a contiguous prop comprising an insulating material as a constituent of the insulating film is disposed. Thus, no cracks form in the insulating interlayer, for example, when a load is applied during wire-bonding.

(2) The present invention described in claim 2 depending on claim 1, wherein the first insulating interlayer and the second insulating interlayer are connected to each other through the openings of the second conductive layer, and a contiguous section of the first insulating interlayer with the second insulating

interlayer is, thereby, formed between the first conductive layer and the third conductive layer.

The provision of the contiguous section (prop) of a hard insulating interlayer is clarified.

In the present invention, openings are selectively provided in a conductive layer which is disposed in an intermediate section, and a contiguous prop is formed by connecting insulating interlayers through the openings, so that the prop carries a load applied to the uppermost layer. No cracks therefore form in the insulating interlayer. As a result, reliability of the semiconductor device improves.

Insulating interlayers of SiO_2 films and the like are generally harder than conductive layers (metal layers). If no openings are formed in the second conductive layer, the first insulating interlayer and the second insulating interlayer are mutually isolated, and each insulating interlayer is sandwiched between two conductive layers. When a load is impressed during wire-bonding, the soft conductive layers are strained, and the strained conductive layers impress the hard insulating interlayers. Cracks will readily form in the hard insulating interlayers disposed between the conductive layers. In contrast, in the present invention, the insulating interlayers can be protected by the contiguous prop and thus crack formation is prevented.

(3) The present invention described in claim 3 depending on claim 1, wherein the second conductive layer has a planar network pattern.

The intermediate conductive layer (the second conductive layer) disposed between the uppermost conductive layer (the first conductive layer) and the lowest conductive layer (the third conductive layer) is shaped into a mesh. Many openings can be effectively formed while maintaining a high current flow density of the second conductive layer.

(4) The present invention described in claim 4 depending on claim 1, wherein the third conductive layer is the lowest conductive layer formed on an insulating film covering a surface of a semiconductor substrate, and the third conductive layer is also provided with a plurality of openings.

Since openings are provided in the lowest conductive layer disposed below the prop of the external connecting terminal, the mechanical strength is further improved and effects for suppressing crack formation in the insulating interlayer is enhanced.

In the openings of the lowest conductive layer (the third conductive layer), the prop of the insulating film is directly connected to the insulating film which covers the surface of the semiconductor substrate, and a hard contiguous prop is formed without disposition of a conductive layer. Since the hard contiguous prop of an insulating film carries the uppermost electrode connected to the external connecting terminal, the strength against a pressure impressed from the upper side is further improved.

(5) The present invention described in claim 5 depending on claim 4, wherein the third conductive layer has a planar network pattern.

The third conductive layer is shaped into a mesh. Many openings can be effectively formed while maintaining a high current flow density of the third conductive layer.

(6) The present invention described in claim 4 depending on claim 1, wherein the conductive member for external connection is a bonding wire.

Cracks will readily form in the insulating interlayer due to an excessive load (impact) applied during wire-bonding. Use of a bonding pad having the above-mentioned structure therefore is effective.

Herein, the external connecting terminal is not limited to the bonding wire and also applicable to

devices using tape carriers and those in which semiconductor chips are directly packaged on substrate using bump electrodes (flip chip packaging). In the present invention, the bonding pad is always planarized regardless of a trend toward multiple layer wiring, the external connecting terminal can be satisfactorily connected.

(7) The present invention described in claim 7 depending on claim 1, wherein the first conductive layer, the second conductive layer and the third conductive layer comprise aluminum as a major component, and the fourth conductive layer and the fifth conductive layer comprise tungsten as a major component.

The fourth and fifth conductive layers comprising tungsten as a major component enables satisfactory embedding.

(8) The present invention described in claim 8 depending on claim 1, wherein the semiconductor device further comprises an internal circuit, the internal circuit being formed by a multiple wiring layer structure; and

the first conductive layer, the second conductive layer, the third conductive layer, the fourth conductive layer, the fifth conductive layer, the first insulating interlayer, the second insulating interlayer, the through holes, and the multiple wiring layer structure are formed by a collective production process.

A complicated production process can be prevented by forming the internal circuit and the connecting section with an external connecting terminal by a collective production process.

(9) The present invention described in claim 9 depending on claim 1, wherein the semiconductor device further comprises guard rings, the guard rings being provided around the multiple wiring layer structure connected to the conductive member for external connection; and

the guard ring comprises:

a sixth conductive layer comprising the same material as the first conductive layer;

a seventh conductive layer comprising the same material as the second conductive layer;

an eighth conductive layer comprising the same material as the third conductive layer;

the first insulating interlayer and the second insulating interlayer;

a first groove provided on the first insulating interlayer;

a second groove provided on the second insulating interlayer;

a ninth conductive layer filled in the first groove; and

a tenth conductive layer filled in the second groove.

If a crack forms in the insulating interlayer, the provided guard ring can prevent the crack from propagating to its circumference. The guard ring can also prevent penetration of water which invades through the bonding wire and the chip. Reliability of the semiconductor device therefore is improved.

(10) The present invention described in claim 10 is a method for making a semiconductor device having a multiple wiring layer structure connected to a conductive member for external connection, comprising the following steps (1) to (7) for forming the multiple wiring layer structure:

Step (1)

forming a first insulating interlayer on a first conductive layer;

Step (2)

selectively forming through holes in the first insulating interlayer;

Step (3)

depositing a first conductive material on the first insulating interlayer and in the through holes and embedding the first conductive material into the through holes by etching the entire surface thereof;

Step (4)

forming a second conductive layer on the first insulating interlayer so as to come into contact with the first conductive material embedded into the through holes;

Step (5)

forming a plurality of openings by patterning the second conductive layer;

Step (6)

forming a second insulating interlayer on the second conductive layer having the plurality of opening;

Step (7)

embedding second conductive material into through holes formed in the second insulating interlayer by the same steps as Step 1 to Step 3; and

Step (8)

forming a third conductive layer on the second conductive layer so as to come in contact with the second conductive material embedded into the through holes.

A technology for forming a multi layer structure in fine semiconductor integrated circuits is also used for forming a bonding pad.

(11) The present invention described in claim 11 depending on claim 10, wherein the second conductive layer, formed in Step (6), having a plurality of openings has a planar network pattern.

The intermediate conductive layer is shaped into a mesh.

(12) The present invention described in claim 12 depending on claim 10, wherein a multiple wiring layer structure constituting an internal circuit of the

semiconductor device is further formed by Step (1) to Step (8).

The multiple wiring layer structure in the internal circuit is also formed by the collective process.

(13) The present invention described in claim 13 depending on claim 10, wherein a guard ring is further formed by Step (1) to Step (8). The guard ring can also be readily formed by the collective process.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is described in detail with reference to the following drawings, wherein like numerals represent like elements and wherein:

Fig. 1 illustrates a structure of a main section in a first embodiment of a semiconductor device;

Fig. 2A is a plan view of the semiconductor device shown in Fig. 1;

Fig. 2B is a cross-sectional view taken from line II(B)-II(B) of Fig. 1;

Fig. 3 is a cross-sectional view of the semiconductor device taken from line III-III of Fig. 2A.

Fig. 4 is a plan view of an intermediate electrode 200 shown in Fig. 1;

Fig. 5 is a cross-sectional view shown in Fig. 3;

Fig. 6A is a plan view of a semiconductor device in accordance with a second embodiment;

Fig. 6B is a cross-sectional view taken from line VI(B)-VI(B) of Fig. 6A;

Fig. 7A is a plan view of a semiconductor device in accordance with a third embodiment;

Fig. 7B is a cross-sectional view taken from line VII(B)-VII(B) of Fig. 7A.

Fig. 8 is a plan view illustrating a modification of the semiconductor device of Fig. 7A.

Fig. 9A is a plan view of a semiconductor device in accordance with a fourth embodiment;

Fig. 9B is a cross-sectional view taken from line IX(B)-IX(B) of Fig. 9A;

Fig. 10 illustrates an arrangement of a bonding pad and an internal circuit in a semiconductor chip;

Fig. 11 is a cross-sectional view illustrating a first step in a method for making a semiconductor device;

Fig. 12 is a cross-sectional view illustrating a second step in a method for making a semiconductor device;

Fig. 13 is a cross-sectional view illustrating a third step in a method for making a semiconductor device;

Fig. 14 is a cross-sectional view illustrating a fourth step in a method for making a semiconductor device;

Fig. 15 is a cross-sectional view illustrating a fifth step in a method for making a semiconductor device;

Fig. 16 is a cross-sectional view illustrating a sixth step in a method for making a semiconductor device;

Fig. 17 is a cross-sectional view illustrating a seventh step in a method for making a semiconductor device;

Fig. 18 is a cross-sectional view illustrating a eighth step in a method for making a semiconductor device;

Fig. 19 is a cross-sectional view illustrating a ninth step in a method for making a semiconductor device;

Fig. 20 is a plan view of a device in accordance with a sixth embodiment;

Fig. 21A illustrates a cross-sectional view of a comparative example;

Fig. 21B illustrates a cross-section of a main section of a semiconductor device;

Fig. 22 illustrates a structure of a modified example of a bonding pad in a semiconductor device; and

Fig. 23 illustrates problems in prior art.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments in accordance with the present invention will now be described with reference to the drawings.

First Embodiment

Figure 1 is a drawing illustrating a configuration of a main section in a first embodiment of a semiconductor device in accordance with the present invention.

As shown in Figure 1, a bonding pad having a triple layer structure comprises a first electrode layer 300, a second electrode layer 200, a third electrode layer 100, a first insulating interlayer 160 provided with a plurality of through holes, conductive members 120a to 120d embedded into the through holes provided in the insulating interlayer 160, a second insulating interlayer 150 provided with a plurality of through holes, and conductive members 110a to 110d embedded into the through holes provided in the insulating interlayer 150. The first electrode layer 300 is formed on an oxide film (insulating film) 410 which covers the surface of the semiconductor substrate.

The bonding wire 180, represented by an alternate long and short dash line in Figure 1, is connected to the uppermost third electrode layer.

Each electrode layer 100, 200, 300 is composed of, for example, aluminum as a major component, and each insulating interlayer is composed of, for example, a SiO_2 film. These layers, however, are not limited to such components, and examples of widely usable insulating interlayers include silicon nitride films (Si_3N_4 films), oxide films containing organic materials, oxide films containing impurities, insulating films comprising organic materials such as polyimides and Teflon, and insulating films formed by superposing two or more types of the above-mentioned insulating films.

The conductive members 110a to 110d and 120a to 120d embedded into the through holes are composed of, for example, tungsten.

The constituents of the electrodes and embedded conductive members are not limited to the above described materials, and various materials are also usable. For example, examples of constituents other than aluminum for each electrode 100, 200, 300 include tungsten, copper, gold, nickel-chromium-titanium, and alloys containing at least one component among these constituents (for example, metal nitride, such as TiN, WN, CuN and AuN; intermetallic compounds, such as Al-Ti, Al-W, Al-Ni and W-Ti; and silicides, such as $TiSi_2$, WSi_2 and $NiSi_2$).

The second electrode layer 200 is provided with a plurality of openings 130a to 130i. The first insulating interlayer 160 and the second insulating interlayer 150 are connected (bonded) to each other through the openings 130a to 130i. As a result, props 140 (shown with a two-dot chain line in Figure 1) comprising the insulating interlayers are formed between the first electrode layer 300 and the second electrode layer 100.

Figures 2A and 2B include a plan view (the upper side) of the bonding pad in Figure 1 and a cross-sectional view (the lower side) taken from line II(B)-II(B). In the plan view, each constituent is described with a solid line for better comprehension in terms of a planar arrangement of each constituent. In Figures 2A-2B, conductive materials embedded into the through holes are described in more detail than Figure 1. Thus, conductive materials referred to as identification numbers 110a, 110b to 117a, and 117b are added.

Figure 3 is a cross-sectional view of the bonding pad taken from line III-III in the plan view in Figure 2A.

Figure 4 shows a planar pattern of the main section of the second electrode layer 200. Figure 4 illustrates that a plurality of openings 130a to 130i are

regularly formed in the second electrode layer 300 in accordance with the present invention, and the second electrode layer 200 has, thereby, a planar network (mesh) pattern. The network pattern is effective in forming many openings while securing a desired current capacity.

As shown in the cross-sectional view (the lower side) of Figure 2B, each of the electrodes 100, 200 and 300 can be extracted and used as wiring layers 102, 202 and 302. The device therefore has a high degree of freedom for the extraction.

As shown Figures 2A and 2B and Figure 3, in this embodiment, the conductive layers 112b to 117b embedded into the through holes in the first insulating interlayer 160 and the conductive layers 112a to 117a embedded into the through holes in the second insulating interlayer 150 are arranged so as to completely overlap in the plan view. This structure is mechanically the most resistive against the vertical stress. The arrangement, however, is not limited to the structure. As shown Figure 5, the first conductive layers 114b, 117b etc. may be slightly shifted from the second conductive layers 114a, 117a etc.

In Figures 2A and 2B and Figure 3, identification number 400 represents a silicon substrate, identification number 410 represents a SiO_2 film covering the entire surface of the silicon substrate. Identification number 240 represents a protecting film.

Advantages in the Embodiment

According to this embodiment, the bonding pad can have a planar shape and has no bumps. When multiple metal electrode layers are formed, the bonding pad can have a planar shape. Disconnection due to bumps therefore will not occur in each layer. Further, the area of the bonding region is constant over all the layers. High density bonding pad arrangement therefore can be achieved.

Also, the second electrode 200 is provided with openings 130a to 130i. and the first insulating

interlayer 160 is connected to the second insulating interlayer 150 through the openings. Props composed of insulating interlayer are, thereby, provided between the first conductive layer and the second conductive layer. Thus, no cracks form in the insulating interlayers 150 and 160 even if a load is applied during wire-bonding.

Insulating interlayers such as SiO_2 films are generally harder than conductive layers e.g. metal layers. If the openings 130a to 130i are not provided in the second electrode 200, the first insulating film 160 and the second insulating film 150 are mutually isolated, and these insulating interlayers are sandwiched between their respective two electrodes (100 and 200, 200 and 300).

A load is applied during wire-bonding, the soft uppermost electrode 100 is distorted, and the distorted electrode 100 impresses the hard insulating interlayer 150. Cracks will readily form in the hard insulating interlayer 150 or 160 which is sandwiched between the two electrodes. The state of crack formation is shown in Figure 21A. In Figure 21A, a stress represented by an arrow is applied, cracks (X and Y) will readily form in the insulating interlayers 150 and 160.

Thus, the openings 130a to 130i are selectively provided in the electrode 200 which is arranged in the center, and the contiguous props (identification number 140 in Figure 1) are formed so as to connecting the insulating interlayers through the openings so that the props carry a load applied to the uppermost electrode layer 100. No cracks therefore form in the insulating interlayers 150 and 160. In the present invention, hard props 140 composed of the insulating interlayer constituent are formed through the openings 130 provided in the second electrode layer 200. Thus, crack formation in the insulating interlayers as shown in Figure 21A can be prevented. As a result, reliability of the semiconductor device is improved.

In the above-mentioned example, openings are provided only in the intermediate electrode (the second electrode layer) among the three electrode layers. The opening arrangement, however, is not limited to this example, and openings may be provided in the first electrode layer (the lowest electrode layer) 300, as shown in Figure 22. In this case, the mechanical strength of the bonding pad is further improved, and crack formation in the insulating interlayers can be further effectively reduced.

As shown in Figure 22, since a plurality of openings 133a to 133i are provided in the first electrode layer 300 so as to overlap with those in the second electrode layer 200, props 142 composed of the insulating interlayer material are directly formed on a insulating film 410 which covers the surface of the semiconductor substrate. Thus, the third electrode layer 100 is supported with hard contiguous props 142 without intervention of a conductive layer. The strength of the bonding pad against a stress applied from the top is further improved.

It is preferable that the first electrode layer 300 be also shaped into a mesh as in the second electrode layer 200. when the first electrode layer 300 is extracted and used as wiring, many openings can be effectively formed while maintaining a high current flow density of the first conductive layer 300.

Openings may be provided in the uppermost electrode layer (the third electrode layer) 100 in which a bonding wire 180 is connected, if necessary.

In the above-mentioned examples, although three electrode layer structures have been described, the present invention is not limited to the three layers of electrode structure, and applicable to two layers, four layers and multiple layers of electrode structure. Thus, the same advantages can be achieved by employing a similar configuration as this embodiment.

Second Embodiment

Figure 6A is a plan view (the upper side) and Figure 6B is a cross-sectional view (the lower side) taken from line VI(B)-VI(B) of the plan view illustrating a configuration in accordance with a second embodiment of the present invention. In Figures 6A and 6B, the open circle represents a conductive layer embedded into through holes in a first insulating interlayer 160, and the black dot represents a conductive layer embedded into through holes in a second insulating interlayer 150.

This embodiment is characterized in that the conductive layers 122, 124, etc., embedded into through holes in the first insulating interlayer 160 do not overlap with the conductive layers 121, 123, etc., embedded into through holes in the second insulating interlayer 150 in the plan view.

The configuration of conductive layers (embedded conductive layers) as shown in this embodiment can also be employed as long as a predetermined current flow capacity is secured.

Third embodiment

Figure 7A is a plan view (the upper side) and Figure 7B is a cross-sectional view (the lower side) taken from line VII(B)-VII(B) of the plan view illustrating a configuration in accordance with a third embodiment of the present invention.

This embodiment is characterized in that a guard ring 500 is provided so as to surround the bonding pad.

As shown in the cross-sectional view of Figure 7B, the guard ring 500 has the same structure as the bonding pad shown in Figure 1 to Figure 3 and comprises conductive layers 302, 502, 508, 506 and 504. The guard ring is formed by the same process as in the bonding pad structure shown in Figure 1 to Figure 3.

If some cracks form in the insulating interlayers 150 and 160, the guard ring 500 can prevent propagation of the cracks to the circumference. The guard ring 500

also prevents penetration of water which enters through the bonding wire 180 or from the circumference of the chip. Reliability of the semiconductor device therefore is improved.

In an example shown in Figure 8, another guard ring 502 is provided outside the guard ring 500. Such a configuration enhances the effects to prevent the crack propagation and water penetration.

Fourth Embodiment

Figure 9A is a plan view (the upper side) and Figure 9B is a cross-sectional view (the lower side) taken from line IX(B)-IX(B) of the plan view illustrating a configuration in accordance with a fourth embodiment of the present invention.

This embodiment is characterized in that conductive layers, which are composed of the same material as the conductive layer for connecting to electrode layers each other in the bonding pad, are embedded instead of providing a guard ring. The same advantages as in the guard ring can be achieved thereby.

In Figures 9A and 9B, identification numbers 612a, 612b, 614a, 614b, 616a, 616b, 618a and 618b represent conductive layers which play the same role as the guard ring. High density arrangement of the conductive layers is preferred in order to enhance the effects for preventing crack propagation and water penetration.

Fifth Embodiment

A manufacturing process of a bonding pad having a configuration as shown in Figure 1 to Figure 4 will now be described.

The bonding pads shown in Figure 1 to Figure 4 are arranged around a semiconductor chip 1000, for example, as shown in Figure 10, and a bonding wire 180 is connected to each bonding pad. In Figure 10, the bonding pad is referred to with identification number 1400. An

internal circuit 1500 is formed in the central section of the semiconductor chip 1000.

Figure 11 is a cross-sectional view taken from line XI-XI in Figure 10. In Figure 11, the left side of the drawing represents a configuration of the bonding pad 1400 and the right side represents a configuration of the internal circuit 1500. The cross-sectional configuration of the bonding pad 1400 corresponds to the cross-sectional configuration shown in Figure 3.

The manufacturing process for the configuration in Figure 11 will now be described step by step with reference to Figure 12 to Figure 17.

As shown in Figure 12, a gate electrode 2018 composed of polysilicon or the like, a p-well layer 2010, and n^+-layers 2012 and 2014 are formed on a semiconductor substrate 2000 to form a MOS transistor. A predetermined electronic circuit is formed thereby.

A contact hole H1 is provided in an insulating film 2500, and a titanium (Ti) film 2100 and a titanium nitride (TiN) film 2120 are deposited step by step on the entire upper surface. The titanium (Ti) film can decrease the contact resistance. The titanium nitride (TiN) film helps embedding of tungsten (W) into the contact hole in the following step.

A tungsten (W) layer 2300 is formed as shown in Figure 13.

Next, as shown in Figure 14, the entire surface of the tungsten layer 2300 is etched with a reactive ion etching (RIE) system to embed tungsten (W) into the contact hole H1. An embedded tungsten layer 2310 is formed thereby. The etching is performed with, for example, a dry etching system at an RF power of 300 W and a vacuum pressure of 240 mTorr using gaseous Ar (90 sccm) as a carrier gas and SF_6 (110 sccm) as an etching gas.

A fluorine gas used for the etching of the tungsten layer in the RIE process generally causes corrosion of aluminum wiring. In the present invention,

however, the bonding pad section and the multiple wiring section of the internal circuit are simultaneously formed, and thus the fluorine gas does not cause corrosion of the electrodes in the bonding pad section. Reliability of the IC chip therefore is improved.

Next, aluminum (Al) and titanium nitride (TiN) are deposited step by step, and the substrate is subjected to a conventional photolithographic process to form aluminum electrodes (3200a and 3200b, 3210a and 3210b) as shown in Figure 15. As shown in Figure 22, when openings 133a to 133i are selectively provided in the first electrode layer of the bonding pad, these openings are formed at predetermined positions in this photographic process for the electrodes (3200a and 3200b, 3210a and 3210b). Herein, the titanium nitride (TiN) films 3210a and 3210b prevent reflection of light during exposure. Namely, the film acts as an antireflection layer.

Next, an insulating interlayer 3000 is formed as shown in Figure 16.

Next, a plurality of through holes are selectively formed in the insulating interlayer 3000 as shown in Figure 17, and a second electrode layer is formed by the same manufacturing process shown in Figure 12 to Figure 15. In Figure 17, identification numbers 3400a and 3400b represent titanium (Ti) films, identification numbers 3410a and 3410b represent titanium nitride (TiN) films, identification numbers 3300, 3302, 3304, 3306, 3308, 3310 represent tungsten (W) layers, identification numbers 4200a and 4200b represent aluminum (Al) films, and identification numbers 4210a and 4210b represent antireflection layers composed of titanium nitride (TiN) films. Openings 130a to 130i as shown in Figure 1 are selectively formed in this step.

As shown in Figure 18, an insulating interlayer 4000 is formed, a plurality of through holes are formed in the insulating interlayer 4000, and a third electrode

layer is formed by the same manufacturing process as in Figure 12 to Figure 15. In Figure 18, identification numbers 3500a and 3500b represent titanium (Ti) films, identification numbers 3510a and 3510b represent titanium nitride (TiN) films, reference numerals 4300, 4302, 4304, 4306, 4308 and 4310 represent tungsten (W) layers, identification numbers 5200a and 5200b represent aluminum (Al) electrodes, and identification numbers 5210a and 5210b represent antireflection layers composed of titanium nitride (TiN) films.

Next, a final protective film 5000 is formed as shown in Figure 19 and a part of the film is selectively opened to form a region for connecting to a bonding wire.

A bonding wire 180 is connected to the third electrode layer to complete the configuration shown in Figure 11.

Sixth Embodiment

Figure 20 is a plan view illustrating a configuration in accordance with a sixth embodiment of the present invention.

This embodiment is characterized in that a first guard ring 500 is provided on the periphery of the bonding pad 1000, and a second guard ring 5500 is provided on the periphery of the semiconductor chip.

As illustrated with reference to Figure 3, the first guard ring 500 prevents the propagation of crack formed in the insulating interlayer in the bonding pad and the penetration of water.

The second guide ring 5500 prevents the penetration of water from the circumference of the semiconductor chip. The semiconductor chip therefore has further improved humidity resistance.

The first guard ring 500, the second guard ring 5500 and the multiple wiring layer structure in the internal circuit 1500 can be produced by a collective production process.

The present invention is widely applicable to substrates using thin films in liquid crystal devices, as well as monolithic ICs. The materials usable for external connection are not limited to the bonding wire and include tape carriers and bump electrodes for direct packaging of semiconductor chips on substrates (flip chip packaging).

While this invention has been described in conjunction with specific embodiments thereof, it is evident that many alternatives, modifications and variations would be apparent to those skilled in the art. Accordingly, preferred embodiments of the invention as set forth herein are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims

WHAT IS CLAIMED IS:

1. A semiconductor device having a multiple wiring layer structure, comprising:

a first conductive layer connected to a conductive member for external connection;

a second conductive layer disposed below said first conductive layer, the second conductive layer having a plurality of openings;

a third conductive layer disposed below said second conductive layer;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

a first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

a second through hole provided in said second insulating interlayer; and

a fifth conductive layer filling said second through hole.

2. The semiconductor device according to claim 1, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of said first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer.

3. The semiconductor device according to claim 1, wherein said second conductive layer has a planar network pattern.

4. The semiconductor device according to claim 1, wherein said third conductive layer is the lowest conductive layer formed on an insulating film covering a surface of a semiconductor substrate, and said third conductive layer is also provided with a plurality of openings.

5. The semiconductor device according to claim 4, wherein said third conductive layer has a planar network pattern.

6. The semiconductor device according to claim 1, wherein said conductive member for external connection is a bonding wire.

7. The semiconductor device according to claim 1, wherein said first conductive layer, said second conductive layer and said third conductive layer comprise aluminum as a major component, and said fourth conductive layer and said fifth conductive layer comprise tungsten as a major component.

8. The semiconductor device according to claim 1, wherein said semiconductor device further comprises an internal circuit, said internal circuit being formed by the multiple wiring layer structure, and said first conductive layer, said second conductive layer, said third conductive layer, said fourth conductive layer, said fifth conductive layer, said first insulating interlayer, said second insulating interlayer, said through holes, and said multiple wiring layer structure are formed by a collective production process.

9. The semiconductor device according to claim 1, wherein said semiconductor device further comprises a guard ring, said guard ring comprising:

a sixth conductive layer comprising the same material as said first conductive layer;

a seventh conductive layer comprising the same material as said second conductive layer;

an eighth conductive layer comprising the same material as said third conductive layer;

said first insulating interlayer and said second insulating interlayer;

a first groove provided on said first insulating interlayer;

a second groove provided on said second insulating interlayer;

a ninth conductive layer filling said first groove; and

a tenth conductive layer filling said second groove.

10. The semiconductor device according to claim 9, wherein said guard ring is formed around said multiple wiring layer structure.

11. The semiconductor device according to claim 9, wherein said guard ring is formed in a perimeter portion of the semiconductor device.

12. The semiconductor device according to claim 1, wherein the first and second through holes are axially aligned.

13. The semiconductor device according to claim 1, wherein the first and second through holes are axially offset.

14. The semiconductor device according to claim 1, wherein the fourth and fifth conductor layers do not overlap.

15. A method for making a semiconductor device having a multiple wiring layer structure connected to a conductive member for external connection, comprising:

(1) forming a first insulating interlayer on a first conductive layer;

(2) selectively forming through holes in said first insulating interlayer;

(3) embedding said first conductive material into said through holes;

(4) forming a second conductive layer on said first insulating interlayer so as to come into

contact with said first conductive material embedded into said through holes;

(5) forming a plurality of openings by patterning said second conductive layer;

(6) forming a second insulating interlayer on said second conductive layer having said plurality of openings;

(7) embedding second conductive material into through holes formed in said second insulating interlayer; and

(8) forming a third conductive layer on said second conductive layer so as to come in contact with said second conductive material embedded into said through holes.

16. The method for making a semiconductor device according to claim 15, further comprising:

depositing said first conductive material on said first insulating interlayer and in said through holes; and

etching said first conductive material.

17. The method for making a semiconductor device according to claim 15, further comprising:

depositing said second conductive material on said first insulating interlayer and in said through holes; and

etching said second conductive material.

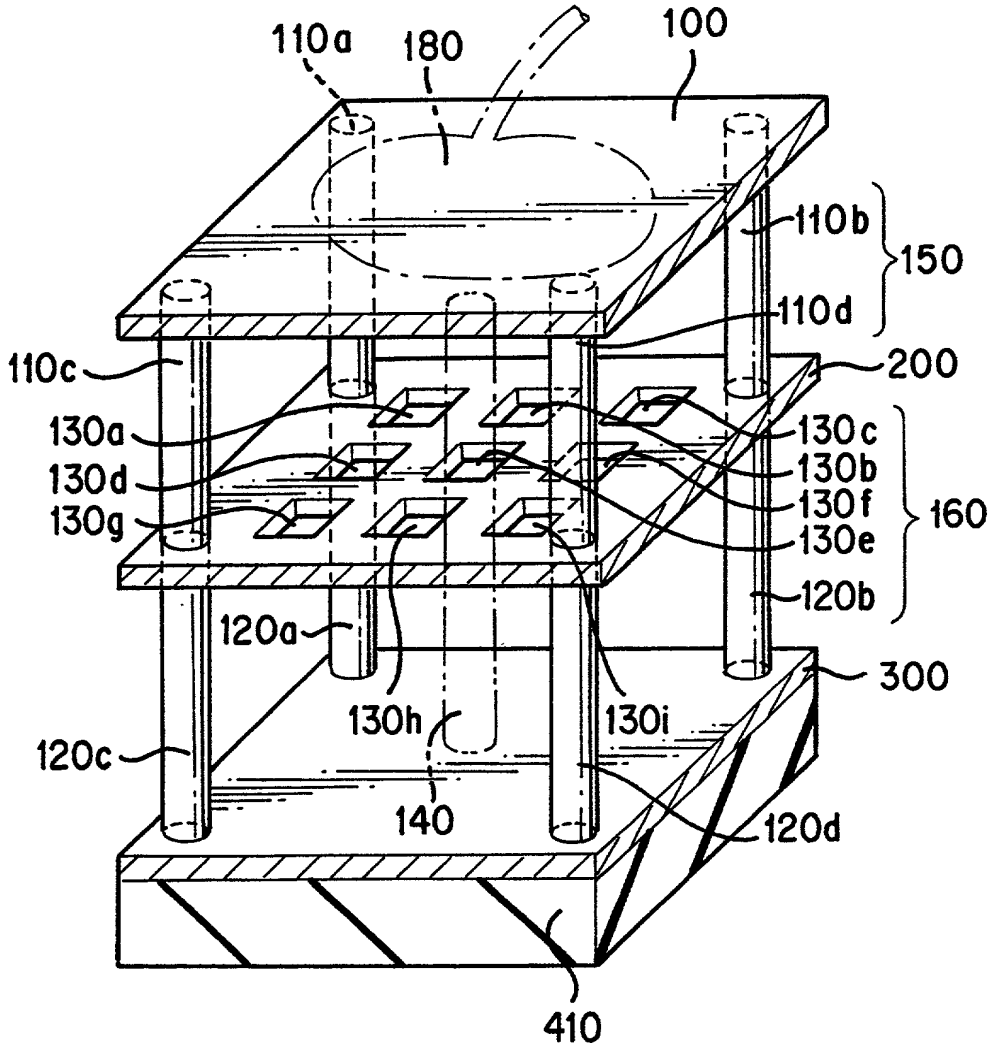
18. The method for making a semiconductor device according to claim 15, wherein said plurality of openings of said second conductive layer forms a planar network pattern.

19. The method for making a semiconductor device according to claim 15, wherein a multiple wiring layer structure of an internal circuit of said semiconductor device is formed by steps (1) to (8).

20. The method for making a semiconductor device according to claim 15, wherein a guard ring is further formed by steps (1) to (8).

ABSTRACT OF THE DISCLOSURE

A semiconductor device and a method for making the same that provide highly reliable and high density arrangement of a connecting region for an external connecting terminal, such as a bonding pad. Electrode layers are connected to each other through embedded conductive layers forming highly-superposed multi-layered structures without bumps. Openings are provided in a second electrode layer, a first insulating interlayer and a second insulating interlayer. The above layers are connected to each other through openings. A prop of the insulating interlayer film is formed between the third electrode layer and the first electrode layer. The props prevent cracks from forming in the insulating interlayers when a load is applied during wire-bonding.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110b
150
110d
110c
200
130a
130d
130g
130c
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120b
120a
300
130h
130i
120c
140
120d
410

FIG. 1

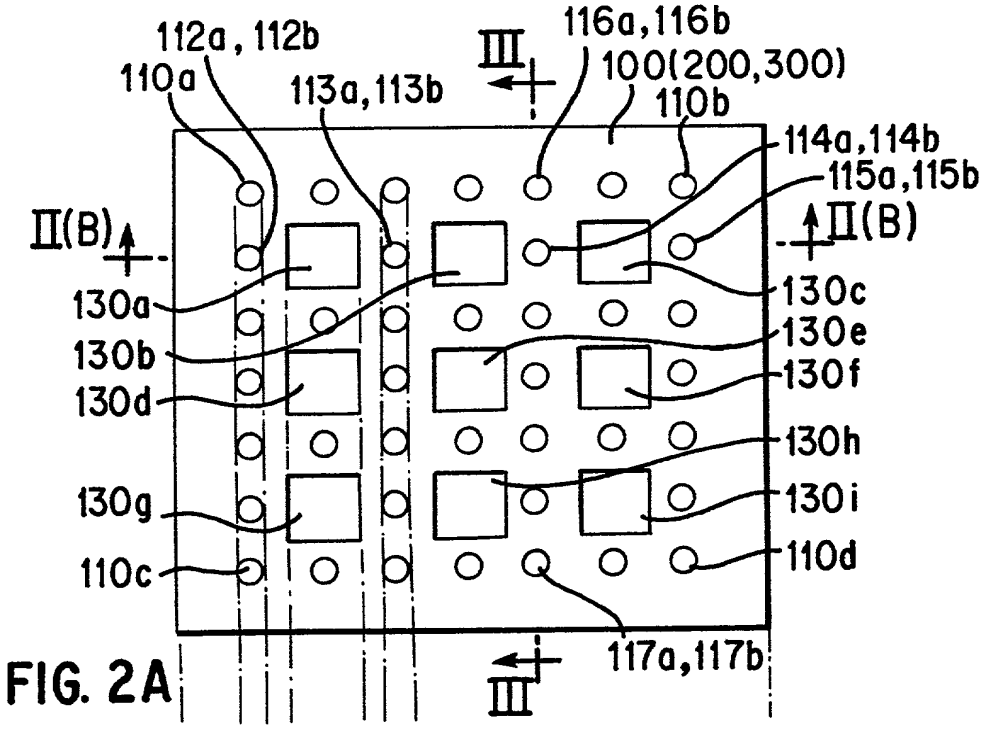
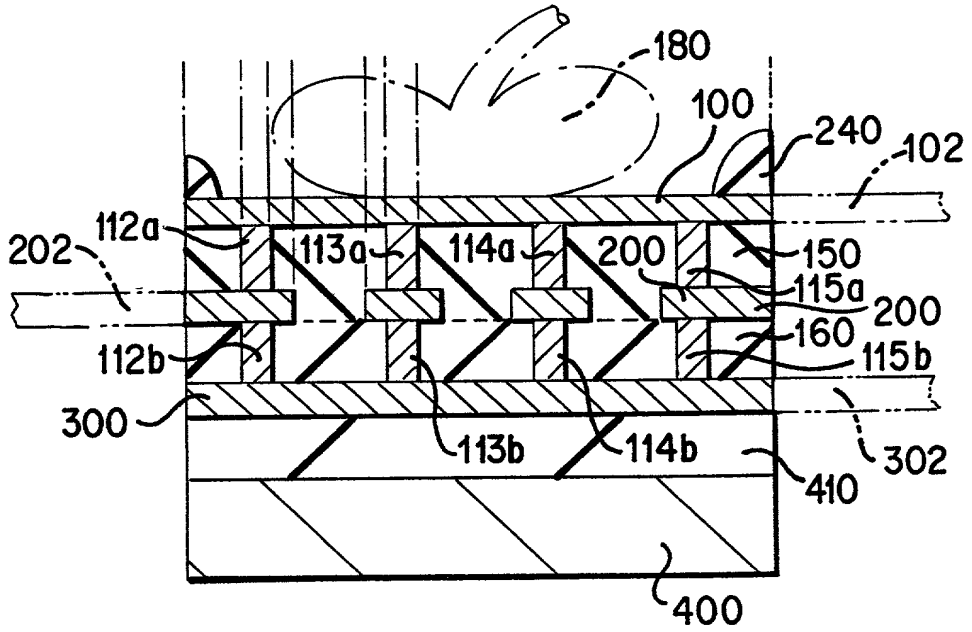

112a, 112b
110a
113a, 113b
III
116a, 116b
100(200,300)
110b
114a, 114b
115a, 115b
II(B)
II(B)
130a
130b
130d
130g
110c
130c
130e
130f
130h
130i
110d
117a, 117b
III

FIG. 2A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100
240
102
112a
202
113a
114a
200
150
115a
200
160
115b
112b
300
113b
114b
302
410
400

FIG. 2B

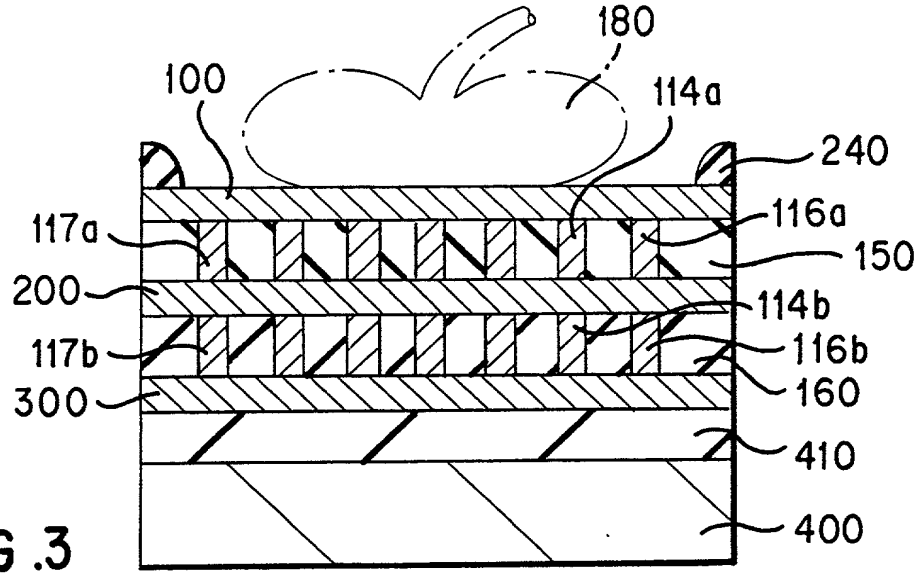


FIG .3

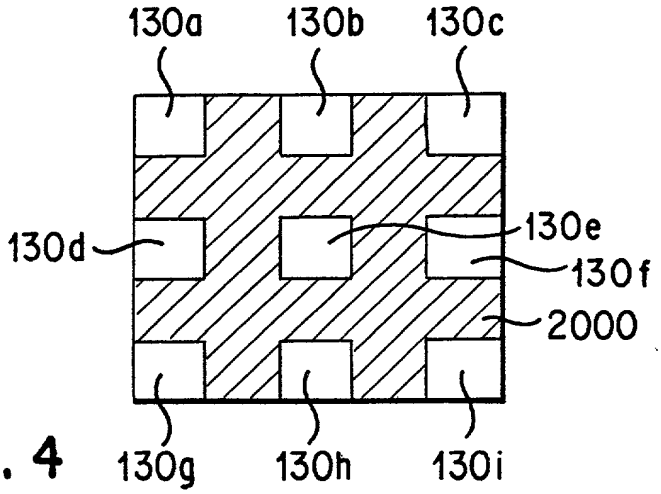


FIG. 4

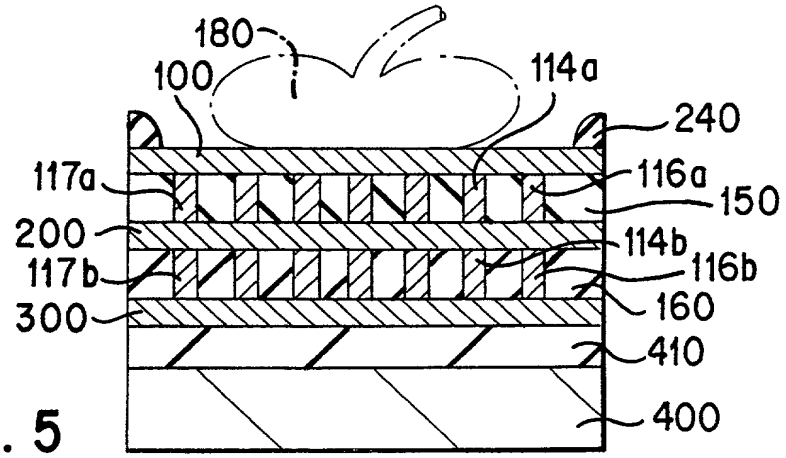


FIG. 5

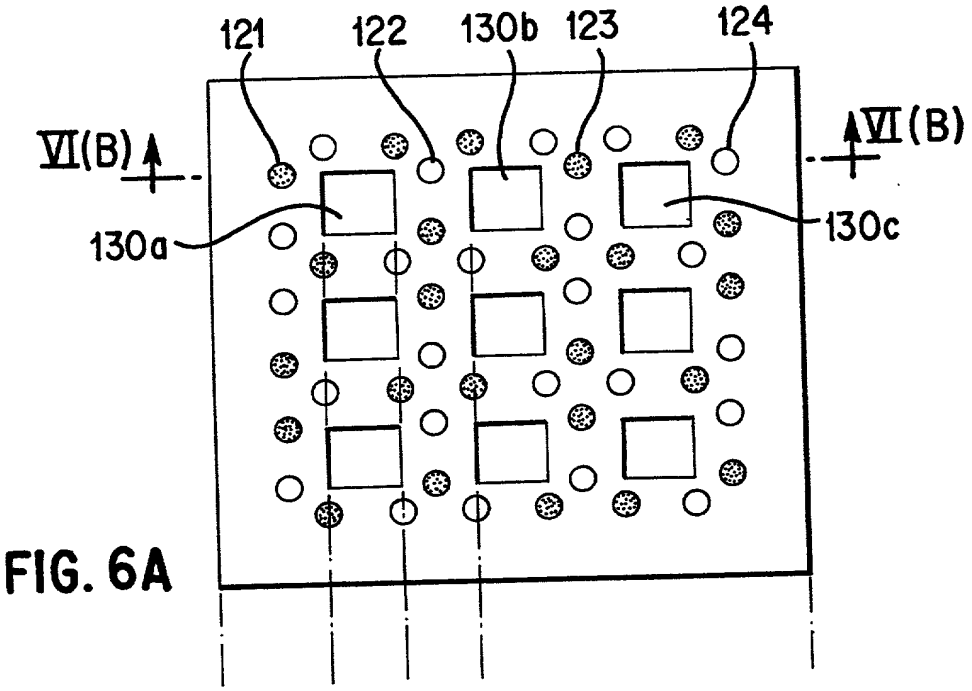
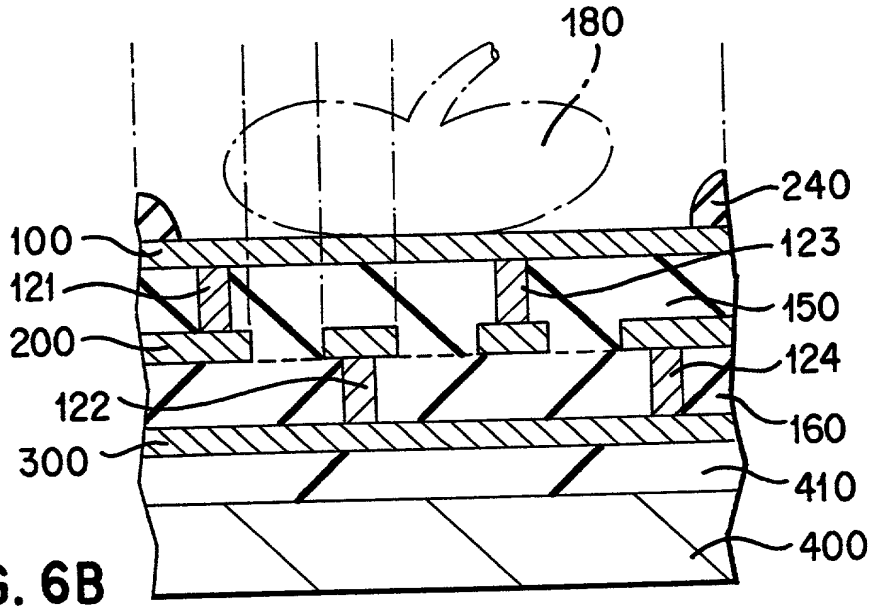

121
122
130b
123
124
VI(B)
VI(B)
130a
130c

FIG. 6A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123
121
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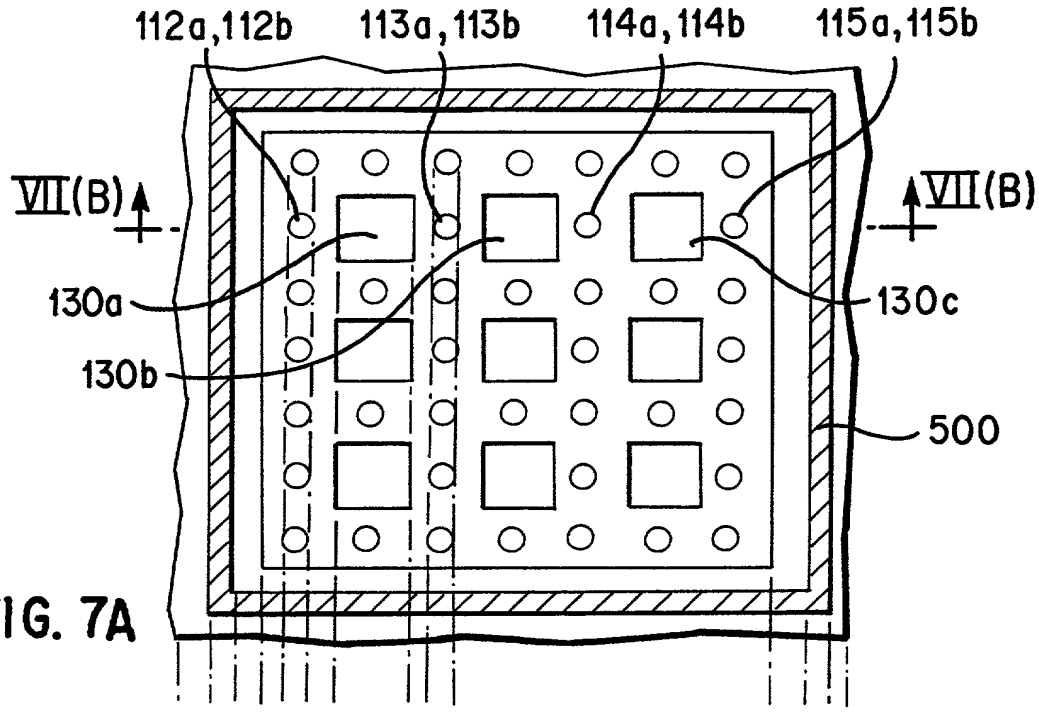
200
124
122
160
300
410
400

FIG. 6B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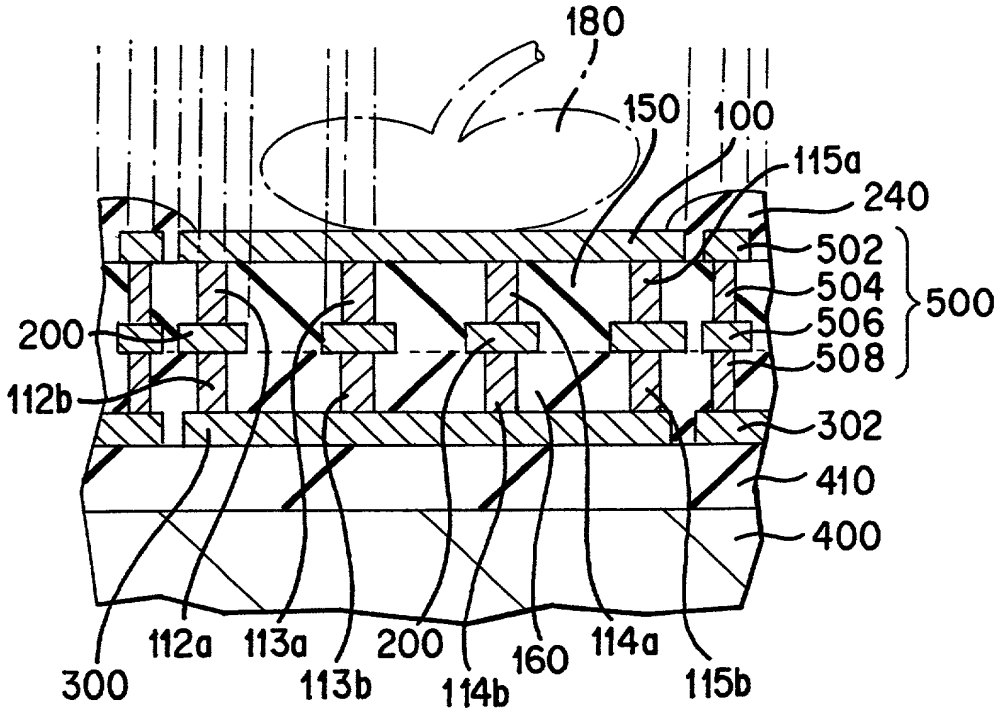
114a,114b
115a,115b
VII(B)
VII(B)
130a
130b
130c
500

FIG. 7A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150
100
115a
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502
504
506
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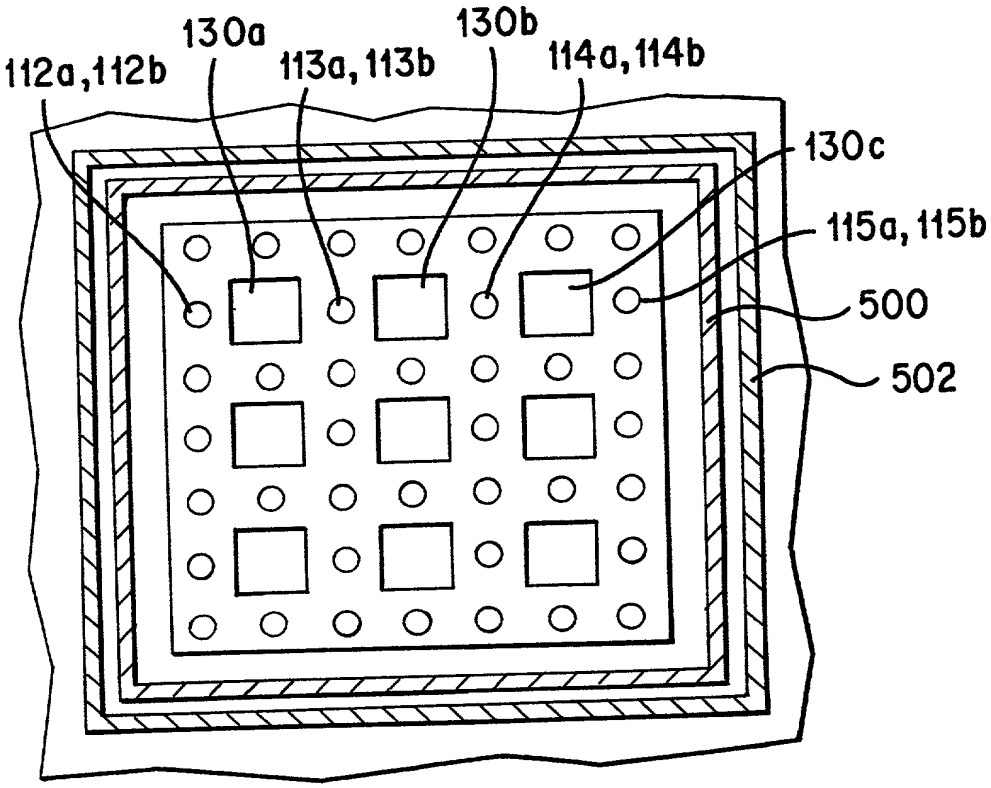
500
200
112b
302
410
400
300
112a
113a
113b
200
114b
160
114a
115b

FIG. 7B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130a
113a,113b
130b
114a,114b
130c
115a,115b
500
502

FIG. 8

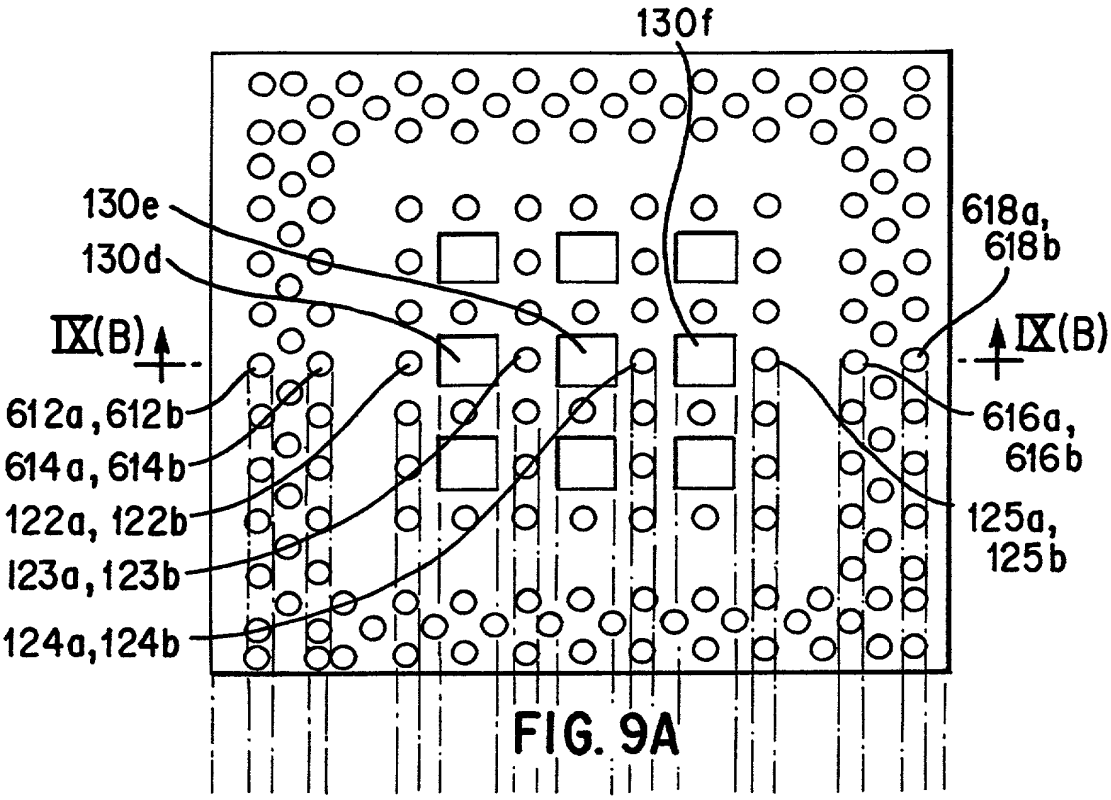
130f
130e
130d
IX(B)
612a,612b
614a,614b
122a, 122b
123a,123b
124a,124b
618a,
618b
IX(B)
616a,
616b
125a,
125b

FIG. 9A

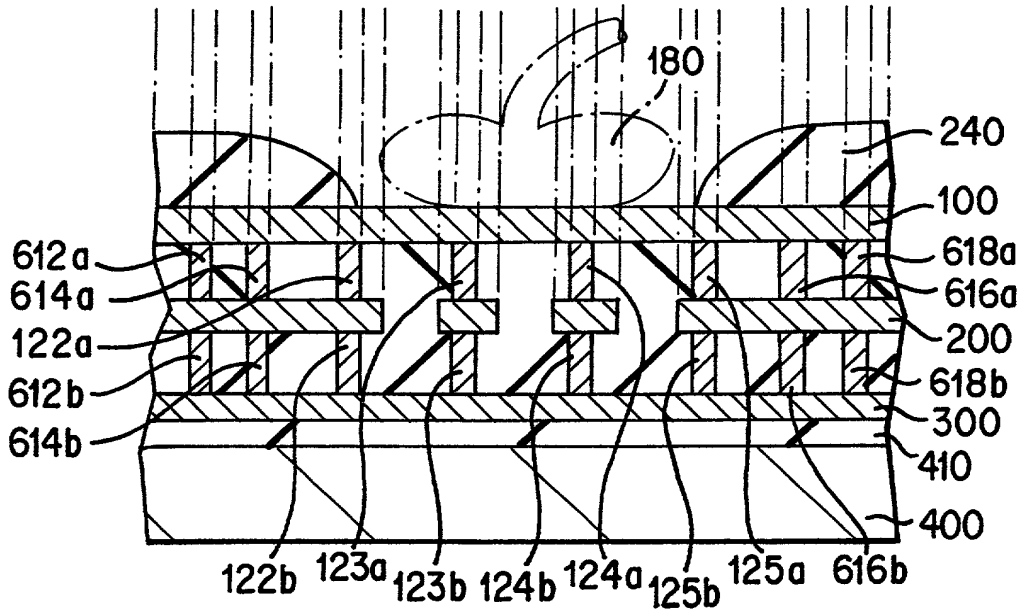
180
240
100
612a
614a
122a
612b
614b
618a
616a
200
618b
300
410
400
122b
123a
123b
124b
124a
125b
125a
616b

FIG. 9B

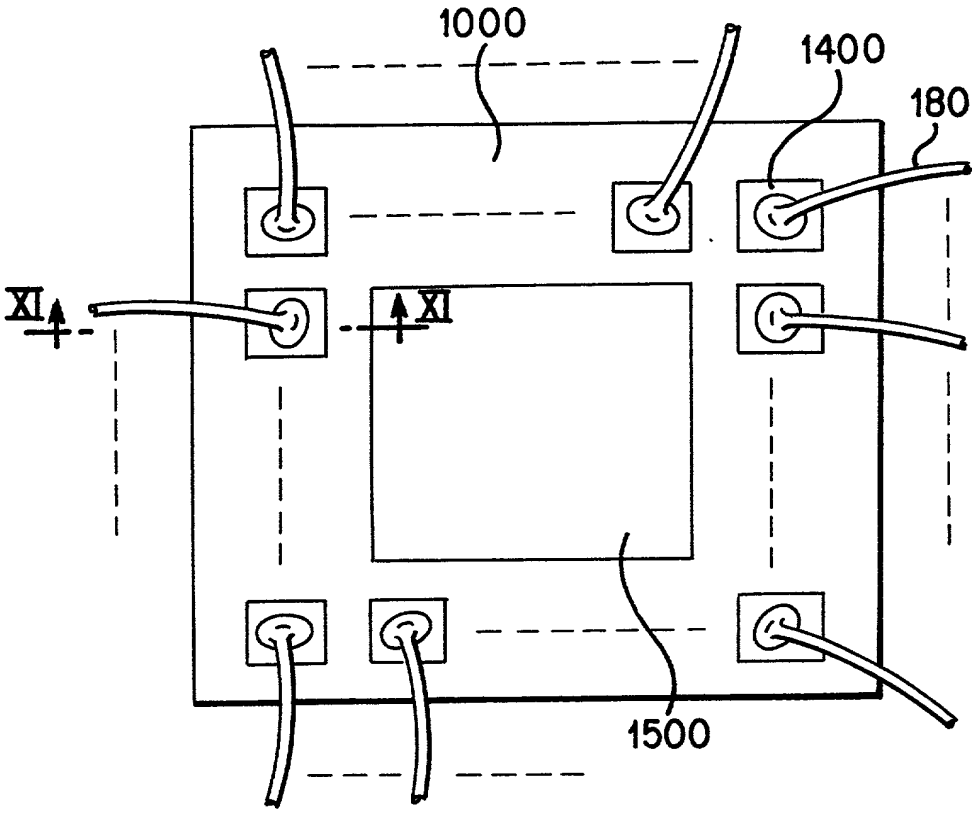

FIG. 10

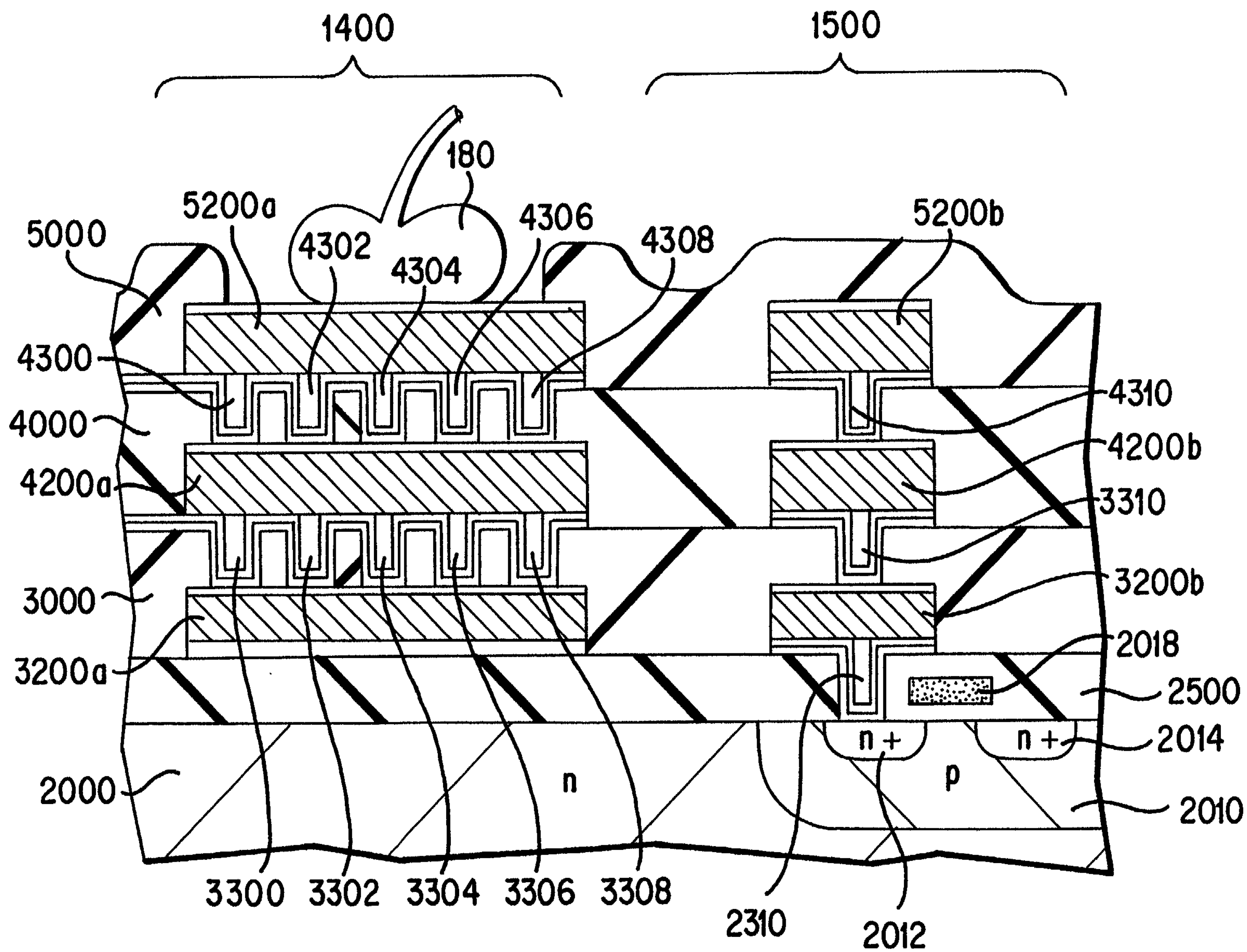
1400
1500
180
5000
5200a
4302
4304
4306
4308
5200b
4300
4000
4200a
3000
3200a
2000
4310
4200b
3310
3200b
2018
2500
2014
2010
n
p
n+
n+
3300
3302
3304
3306
3308
2310
2012

FIG. 11

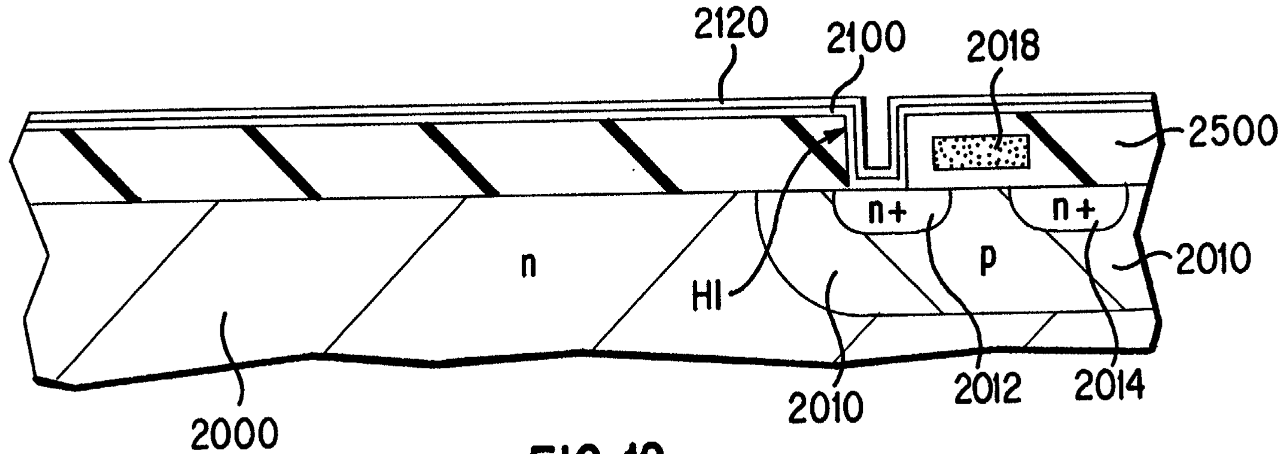
2120
2100
2018
2500
n+
n+
n
p
HI
2010
2000
2010
2012
2014

FIG. 12

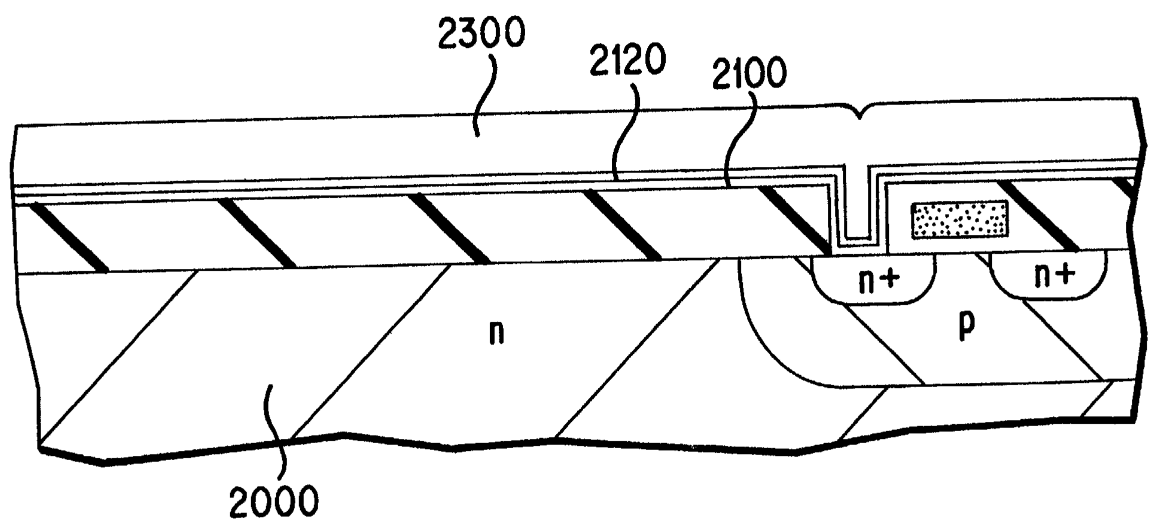
2300
2120
2100
n+
n+
n
p
2000

FIG. 13

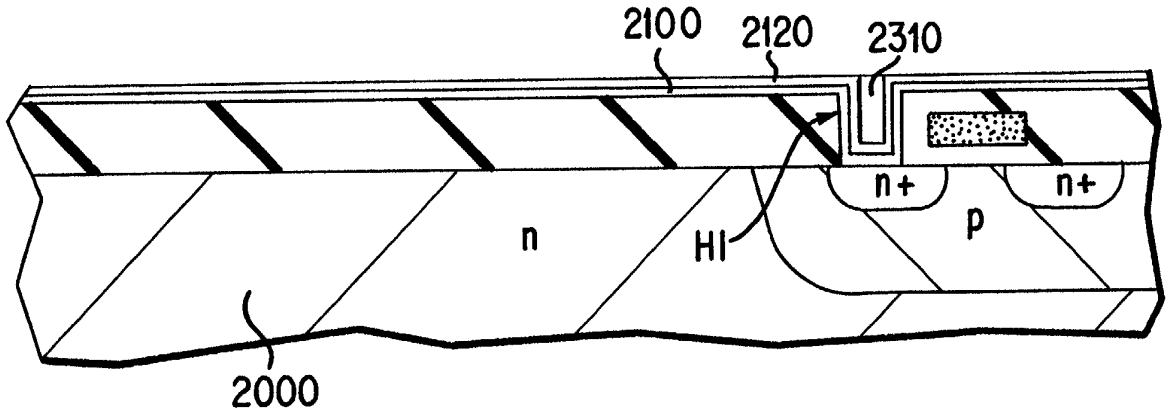
2100
2120
2310
n+
n+
n
HI
p
2000

FIG. 14

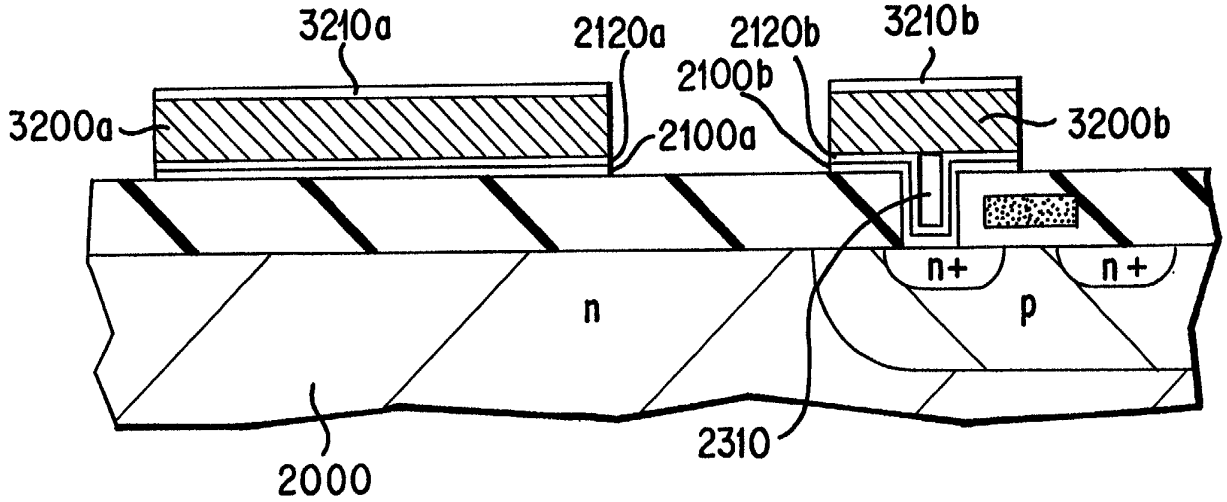
3210a
2120a
2120b
3210b
2100b
3200a
2100a
3200b
n+
n+
n
p
2000
2310

FIG. 15

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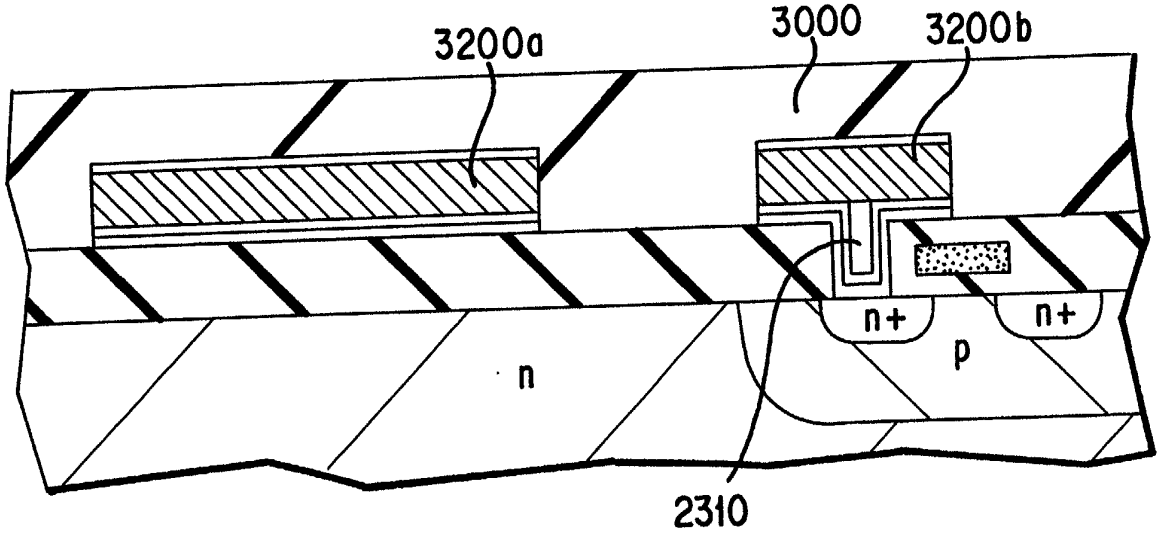


FIG. 16

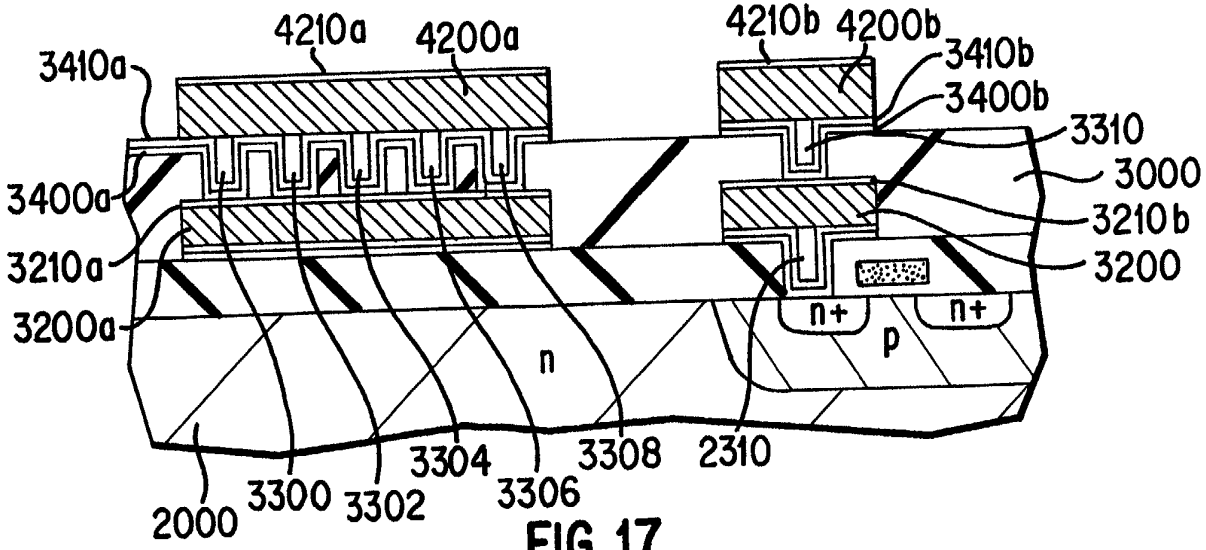
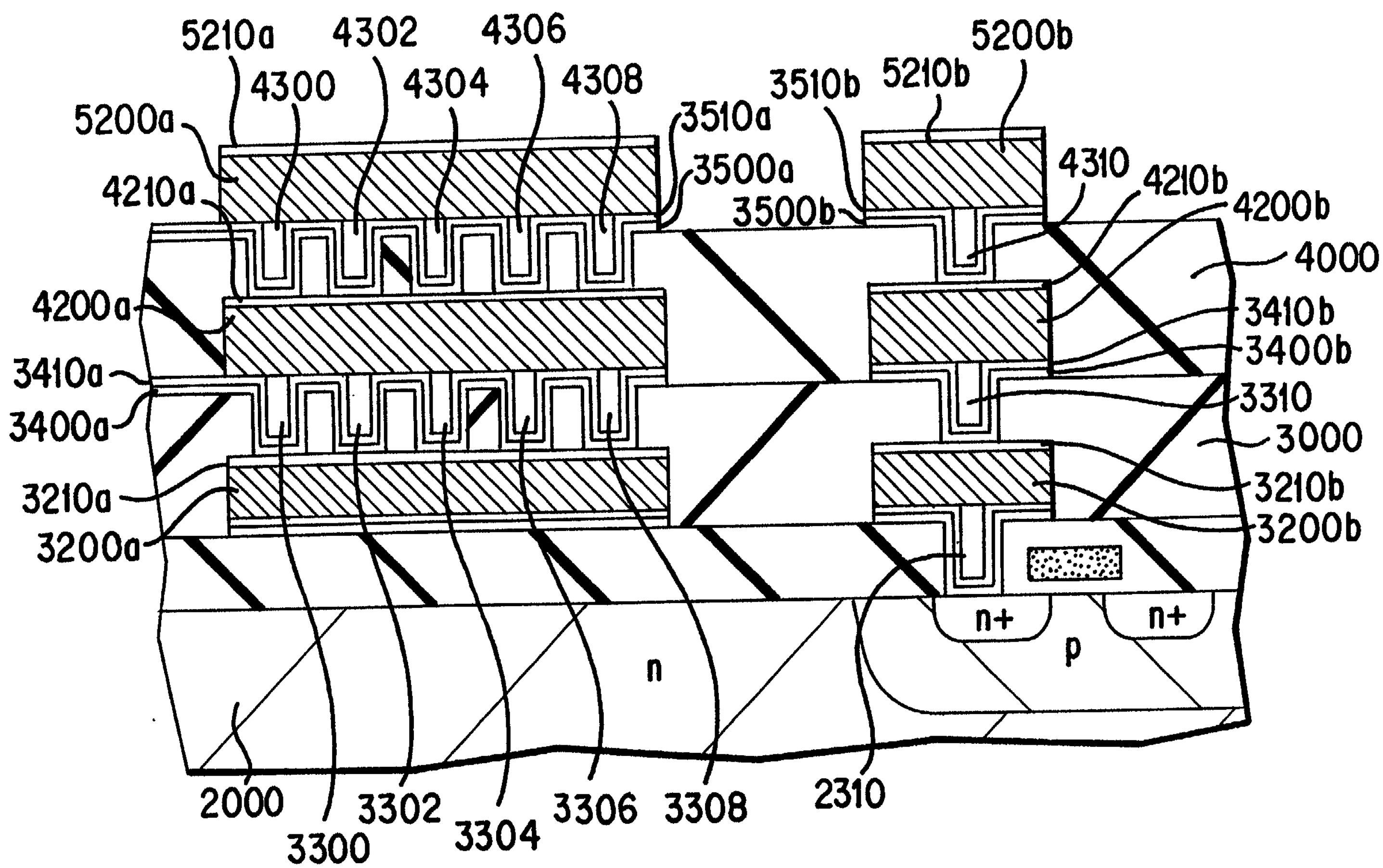


FIG. 17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4306
4300
4304
4308
5200a
3510a
3510b
5210b
5200b
3500a
4210a
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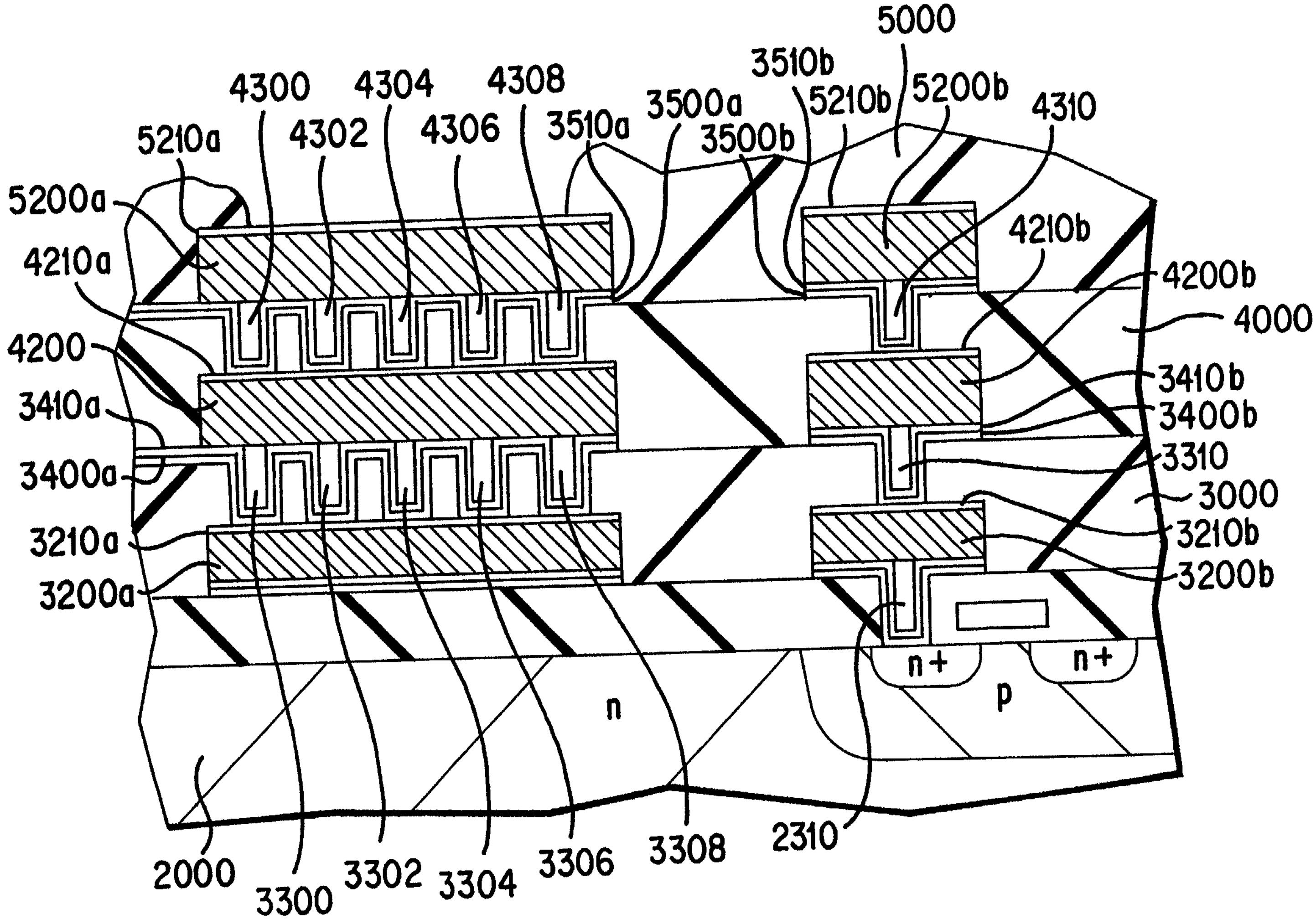
4310
4210b
4200b
4000
4200a
3410b
3400b
3410a
3310
3400a
3000
3210a
3210b
3200a
3200b
n+
n+
p
n
2000
3300
3302
3304
3306
3308
2310

FIG. 18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5210b
5200b
4310
4300
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4308
4302
4306
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3500a
3500b
5210a
5200a
4210a
4210b
4200b
4000
4200
3410b
3410a
3400b
3310
3400a
3000
3210a
3210b
3200b
3200a
n+
n+
p
n
2000
3300
3302
3304
3306
3308
2310

FIG. 19

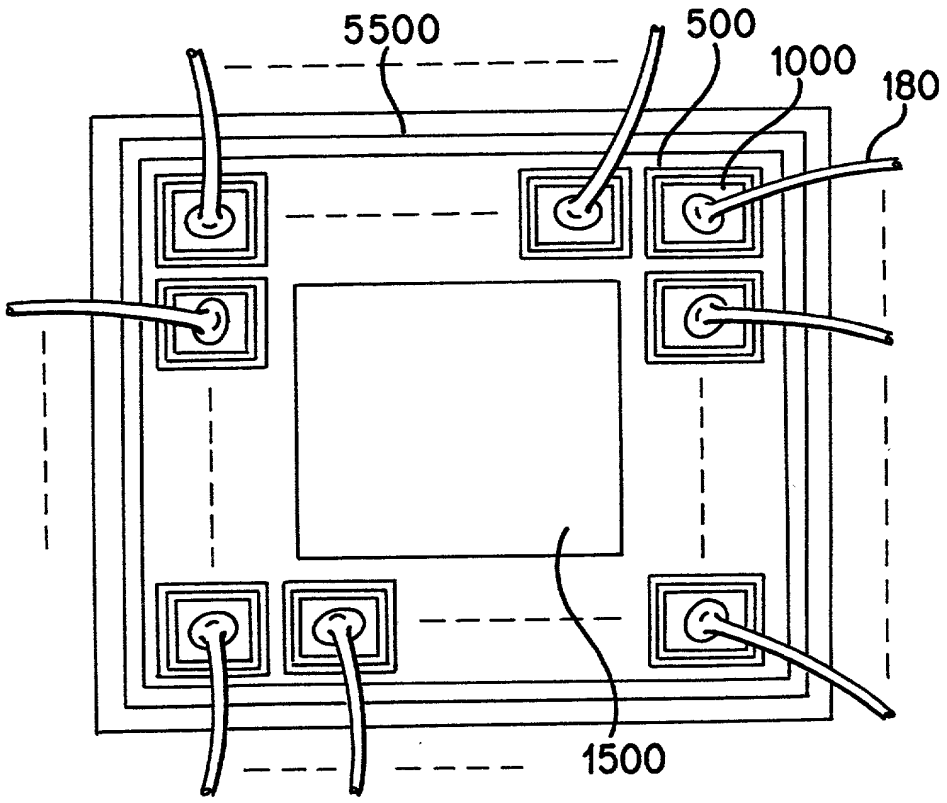

FIG. 20

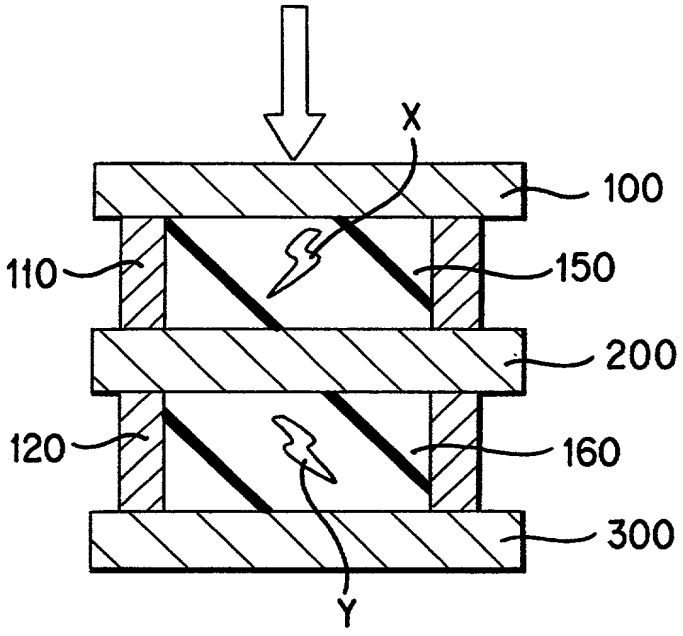

FIG. 21A

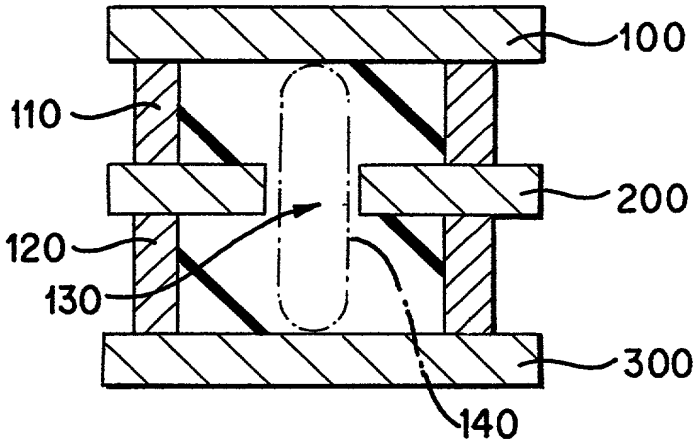

FIG. 21B

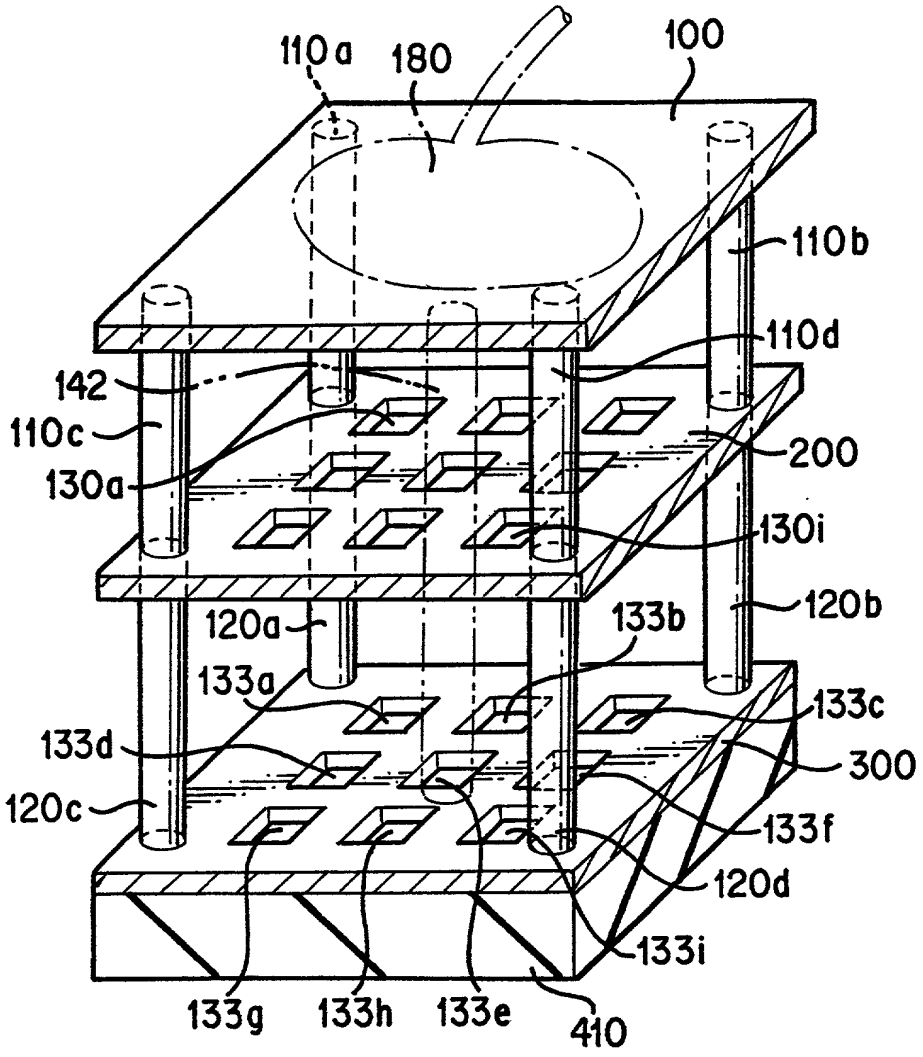
110a
180
100
110b
110d
142
110c
130a
200
130i
120a
133b
120b
133a
133c
133d
300
120c
133f
120d
133i
133g
133h
133e
410

FIG. 22

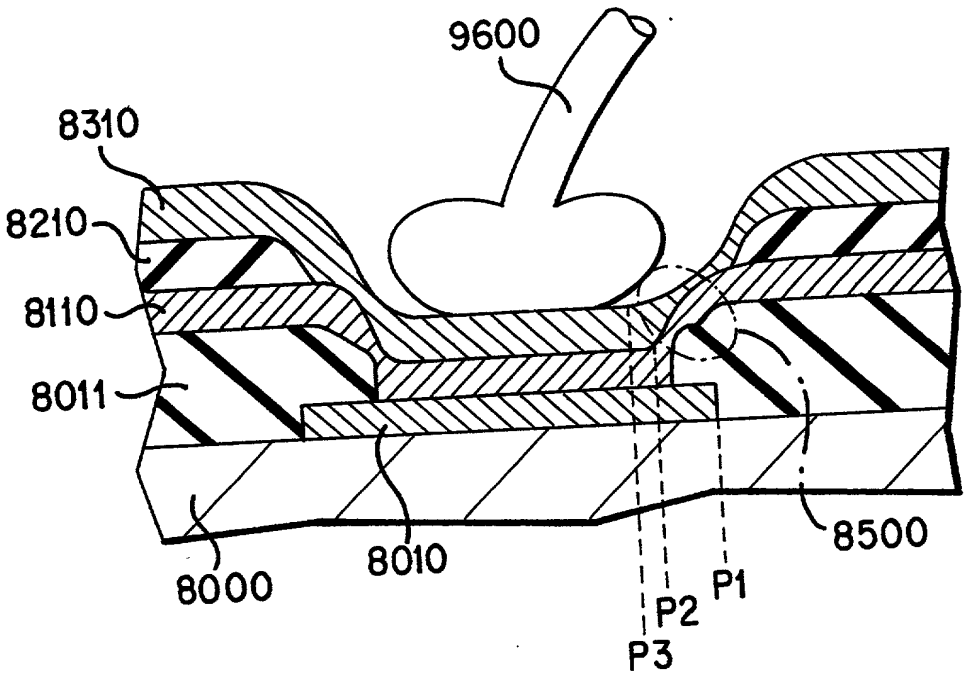

FIG. 23 PRIOR ART

Docket No.: JAO 39894

APPLICATION FOR UNITED STATES PATENT DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME

described and claimed in the specification:

Check one

*a. ☐ attached hereto.

b. ☒ filed on August 19, 1997 as Application No. 08/914,095.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

Under Title 35, U.S. Code §119, the priority benefits of the following foreign application(s) and/or United States provisional application(s) filed within one year prior to this application are hereby claimed:

Japanese Patent Application No. 8-237310 filed August 20, 1996

The following application(s) for patent or inventor's certificate on this invention were filed in countries foreign to the United States of America either (a) more than one year prior to this application, or (b) before the filing date of the above-named foreign priority application(s) and/or United States provisional application(s):

I hereby appoint the following as my attorneys of record with full power of substitution and revocation to prosecute this application and to transact all business in the Patent Office:

James A. Oliff, Reg. No. 27,075; William P. Berridge, Reg. No. 30,024; Kirk M. Hudson, Reg. No. 27,562; Thomas J. Pardini, Reg. No. 30,411; Edward P. Walker, Reg. No. 31,450; Robert A. Miller, Registration No. 32,771 and Mario A. Costantino, Registration No. 33,565.

ALL CORRESPONDENCE IN CONNECTION WITH THIS APPLICATION SHOULD BE SENT TO OLIFF & BERRIDGE, P.O. BOX 19928, ALEXANDRIA, VIRGINIA 22320, TELEPHONE (703) 836-6400.

I hereby declare that I have reviewed and understand the contents of this Declaration, and that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1 ***Typewritten Full Name of First or Sole Inventor*** Kazuo (Given Name) — Middle Initial — TANAKA (Family Name)

2 **Inventor's Signature: [signature]

3 **Date of Signature: Jan (Month) 29 (Day) 1998 (Year)

Residence: Suwa-Shi, Nagano-ken (City) — (State or Province) — JAPAN (Country)

Citizenship: Japanese

Post Office Address: (Insert complete mailing address, including country) c/o Seiko Epson Corporation, 3-5 Owa 3-chome, Suwa-shi, Nagano-ken 392, JAPAN

*If Box (a.) is checked, this form may be executed only when attached to the specification (including claims).

**Note to Inventor: Please sign name exactly as it appears above and insert actual date of signing.

IF THERE IS MORE THAN ONE INVENTOR USE PAGE 2 AND PLACE AN "X" HERE ☐

10/96